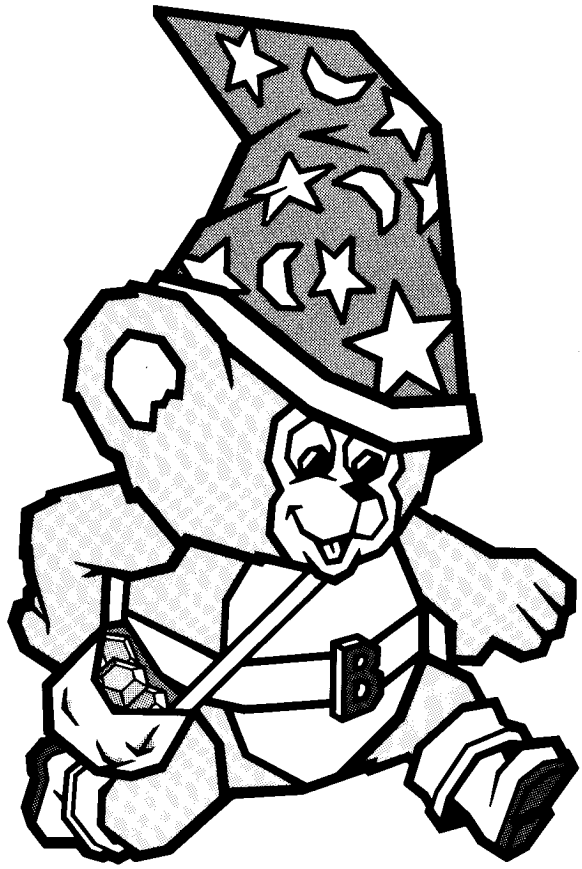

NOTE
Remove this staple to separate the schematic diagrams from the Troubleshooting Guide.

Schematic Package Supplement to

CRYSTAL CASTLES™

Operators Manual

Includes
Troubleshooting Guide

7M

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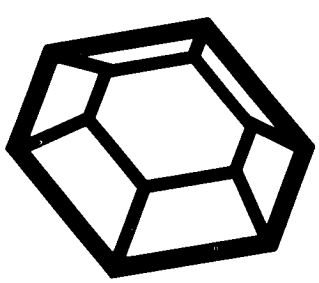
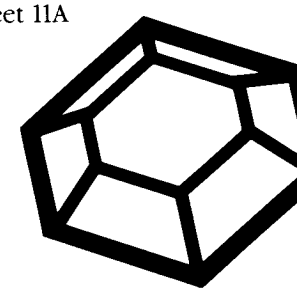
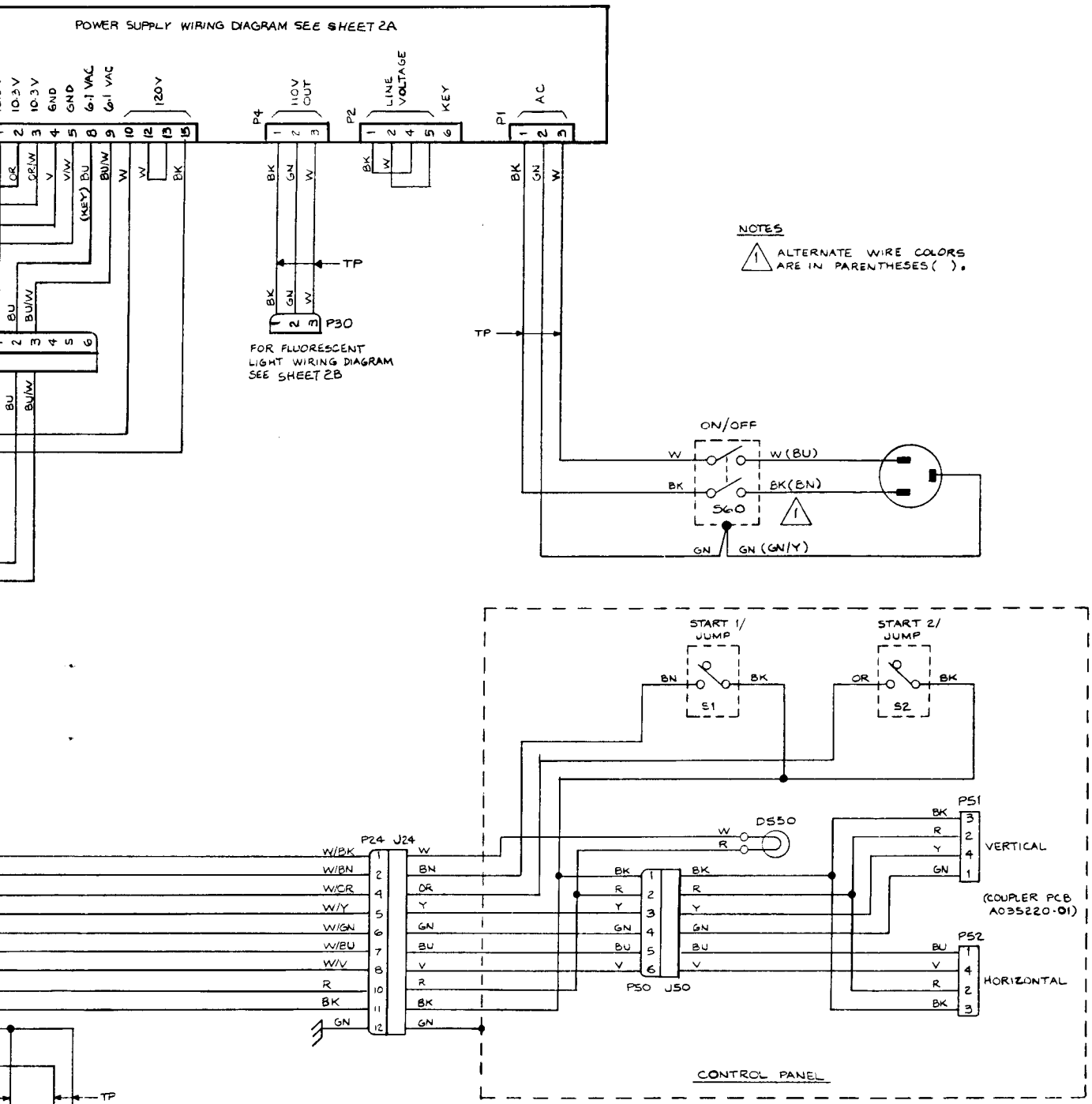


NOTE

A Crystal Castles Troubleshooting Guide is included as part of this Schematic Package Supplement. The Troubleshooting Guide contains Atari CAT Box troubleshooting procedures.





Crystal Castles Main Wiring Diagram

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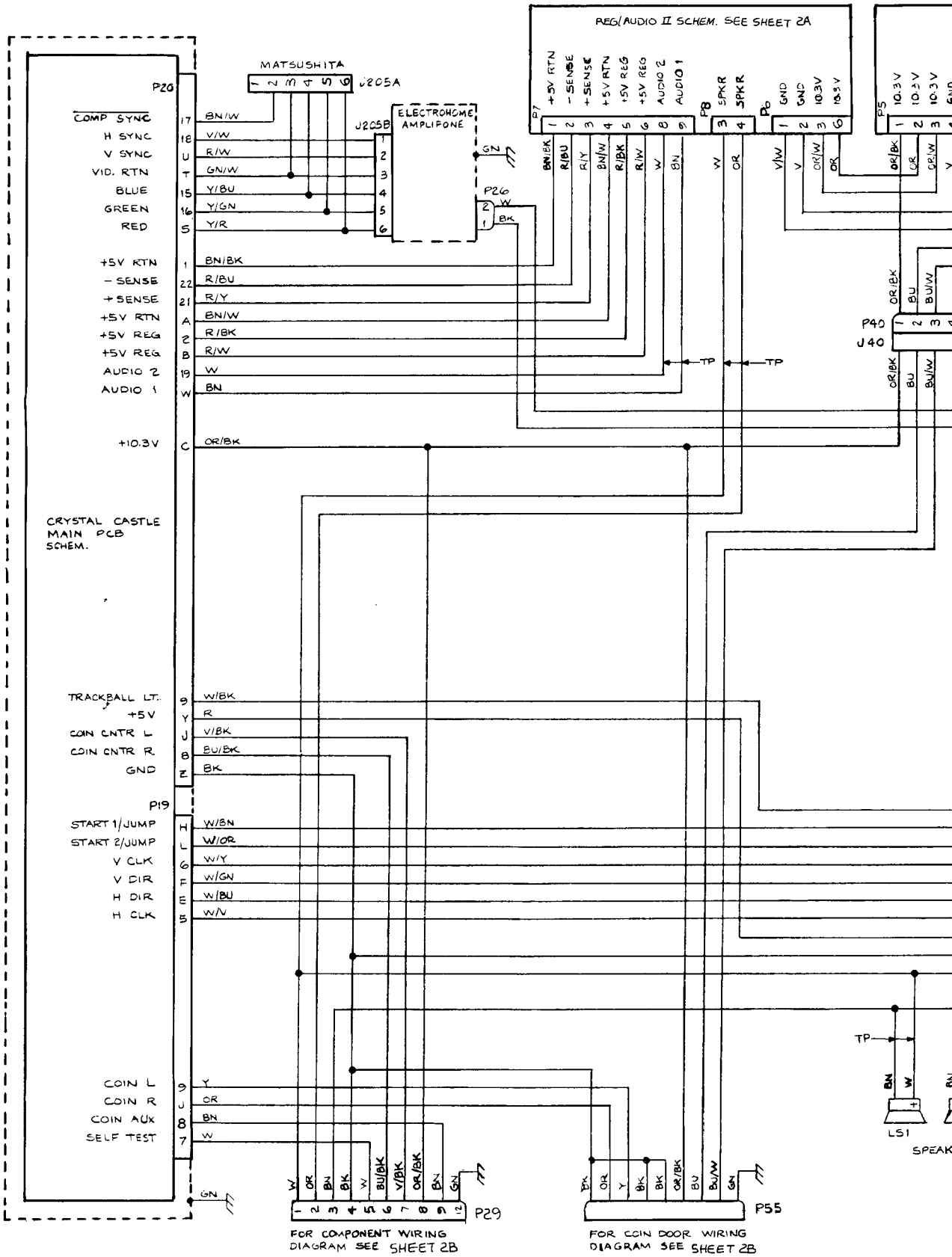
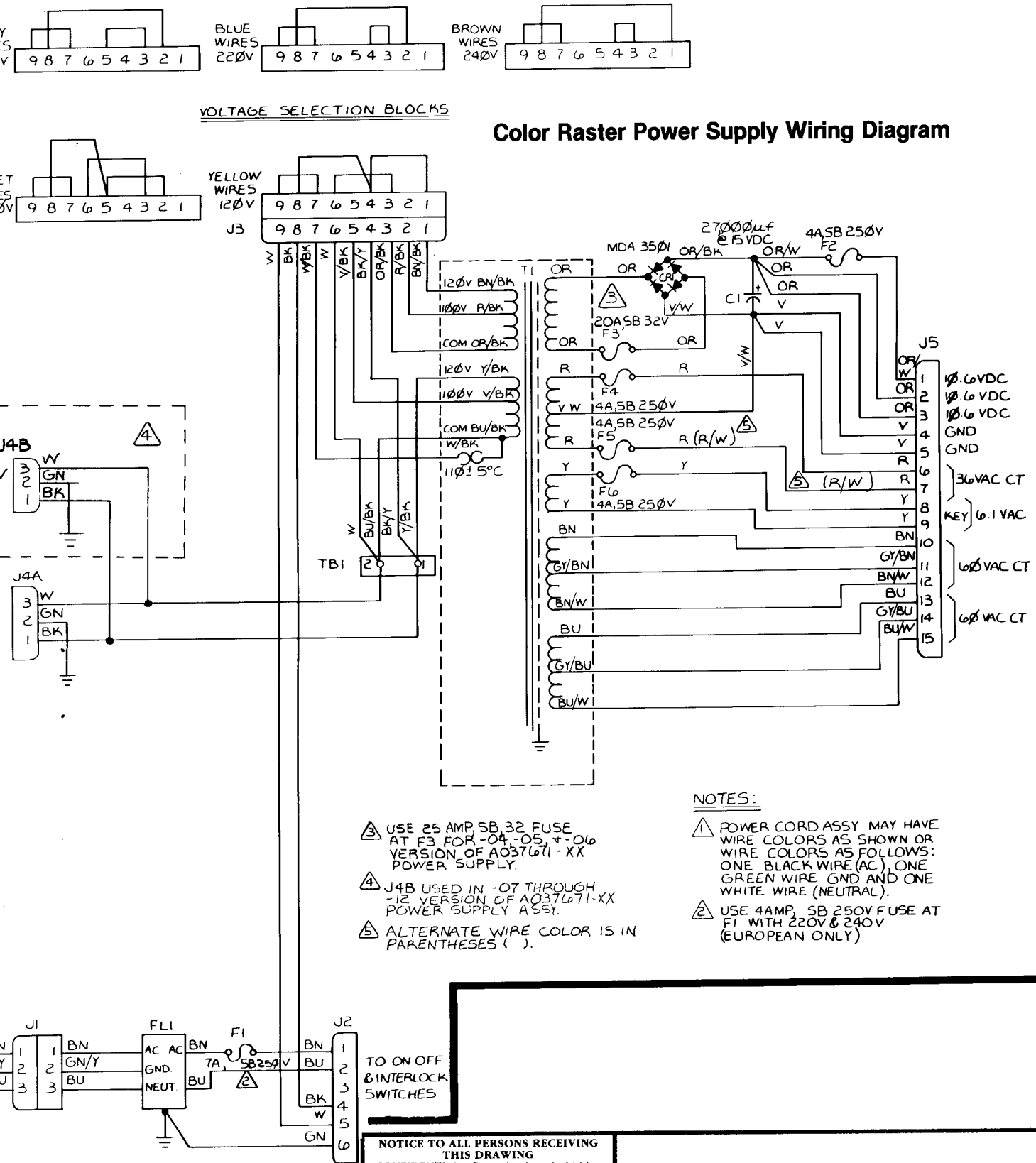

REG/AUDIO II SCHEM. SEE SHEET 2A
MATSUSHITA
J205A
ELECTROHOME AMPLIFONE
J205B
P26
P20
COMP SYNC
H SYNC
V SYNC
VID. RTN
BLUE
GREEN
RED
+5V RTN
– SENSE
+SENSE
+5V RTN
+5V REG
+5V REG
AUDIO 2
AUDIO 1
+10.3V
CRYSTAL CASTLE MAIN PCB SCHEM.
TRACKBALL LT.
+5V
COIN CNTR L
COIN CNTR R
GND
P19
START 1/JUMP
START 2/JUMP
V CLK
V DIR
H DIR
H CLK
COIN L
COIN R
COIN AUX
SELF TEST
P7
P8
P6
P5
P40
J40
TP
LS1
P29
P55
FOR COMPONENT WIRING DIAGRAM SEE SHEET 2B
FOR COIN DOOR WIRING DIAGRAM SEE SHEET 2B



Color Raster Power Supply Wiring Diagram

NOTES:

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE GND AND ONE WHITE WIRE (NEUTRAL).
2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY)
3. USE 25 AMP SB 32 FUSE AT F3 FOR -04, -05, & -06 VERSION OF A037671-XX POWER SUPPLY.
4. J4B USED IN -07 THROUGH -12 VERSION OF A037671-XX POWER SUPPLY ASSY.
5. ALTERNATE WIRE COLOR IS IN PARENTHESES ( ).

Crystal Castles Regulator/Audio II PCB and Power Supply Diagrams

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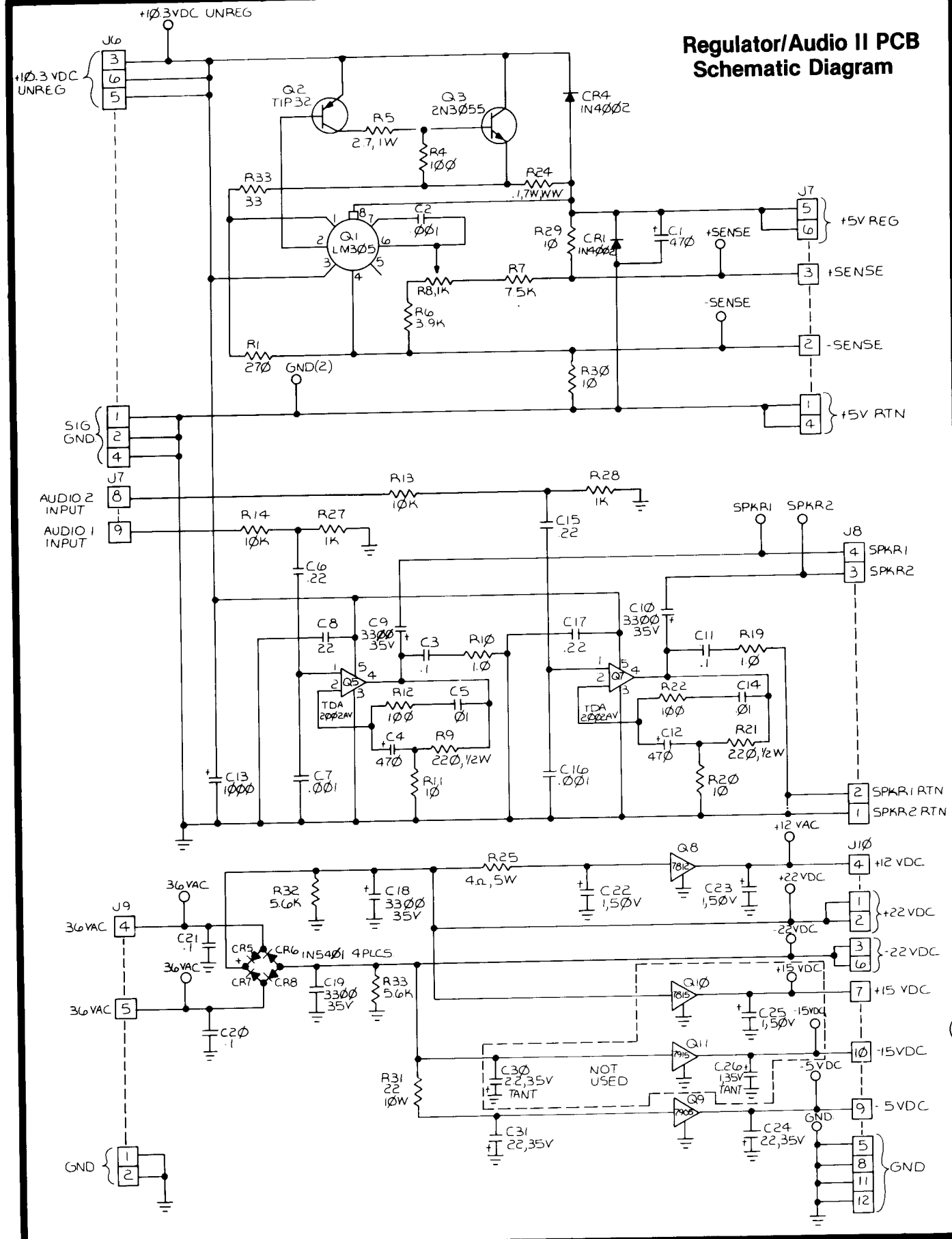
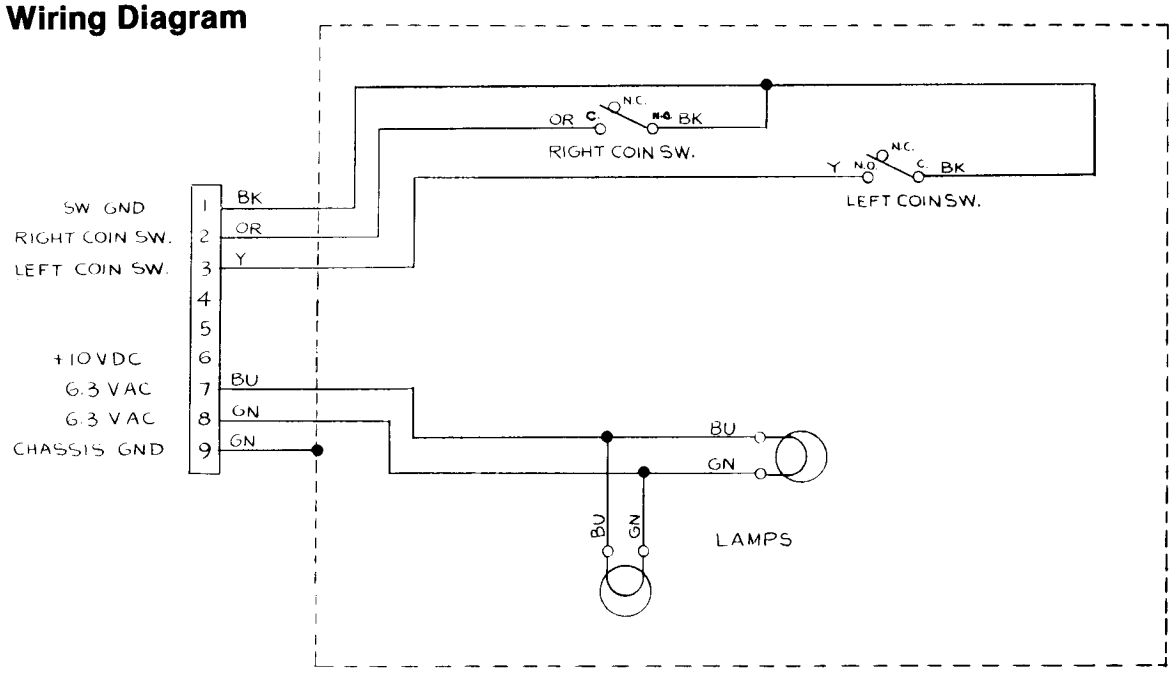
Regulator/Audio II PCB Schematic Diagram



Coin Door Wiring Diagram



Crystal Castles Game Interfaces

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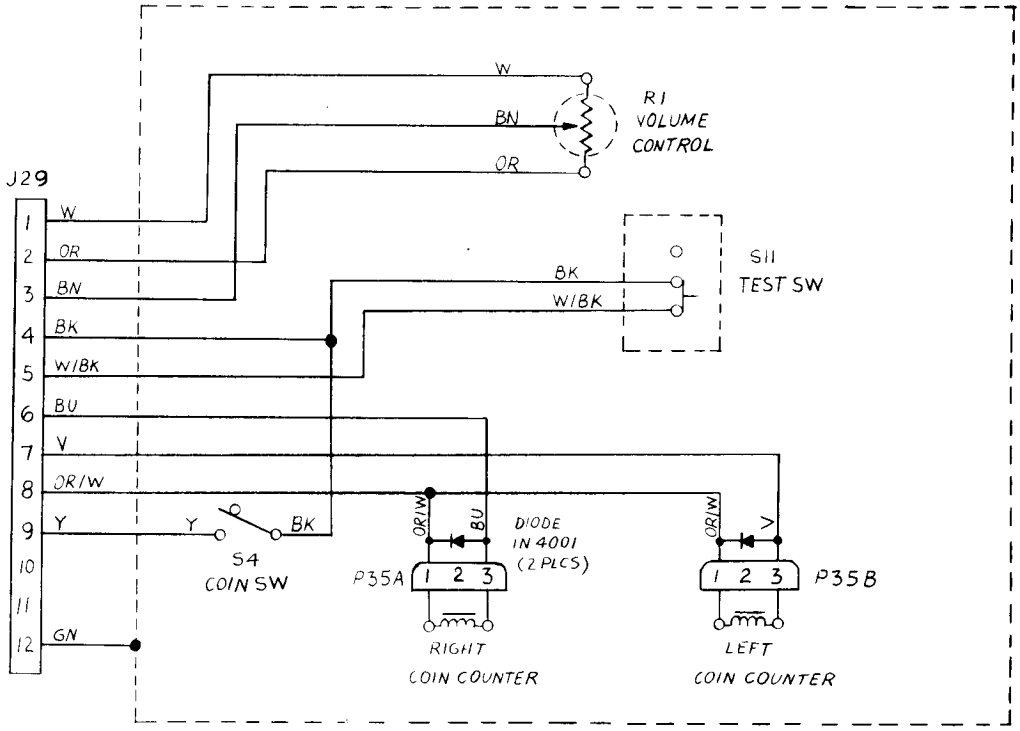
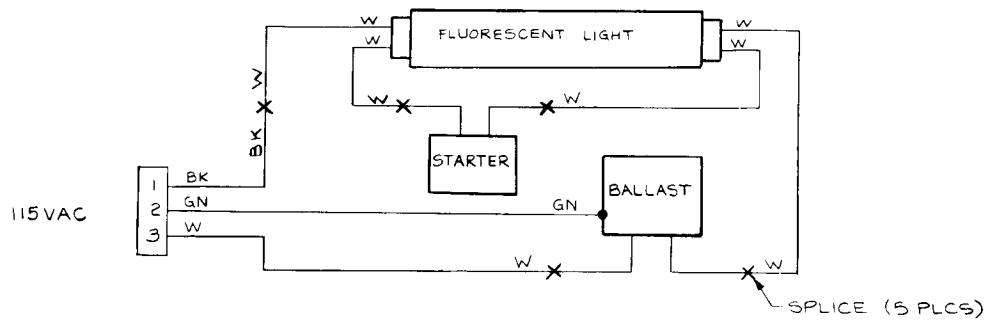
Utility Panel Wiring Diagram



Fluorescent Light Wiring Diagram



00	**FUNCTION**
X	X COORDINATE
D	Y COORDINATE
	BIT MODE
D	WORKING RAM (DRAM)
D	SCREEN RAM
D	WORKING RAM (STATIC)
D	MOTION OBJECT BUF 2
D	MOTION OBJECT BUF1
D	MOTION OBJECT PICTURE
D	MOTION OBJECT VERTICAL
	MOTION OBJECT PRIORITY
D	MOTION OBJECT HORIZONTAL
D	NOVRAM
	TRAK-BALL
	IN0
D	COIN R
	COIN L
	COIN AUX
	SLAM
	SELF TEST
	SPARE
	JMP 1
	JMP 2
D	CI/O 0
D	CI/O 1
D	OPTION SW
	SPARE
	SPARE
	COCKTAIL
	RECALL
D	HOR SCROLL CNTR LOAD
D	VERT SCROLL CNTR LOAD
	INTERRUPT ACKNOWLEDGE
	WDOG
D	OUT 0
D	TRAK-BALL LIGHT
D	
D	STORE LOW
D	STORE HIGH
D	SPARE
D	COIN CNTR R
D	COIN CNTR L
D	BANK0–BANK 1
	OUT 1
	$\overline{AX}$
	$\overline{AY}$
	$\overline{XINC}$
	$\overline{YINC}$
	PLAYER 2
	$\overline{SIRE}$
	BOTHRAM
	BUF1/$\overline{BUF2}$
D	COLORAM
D	PROGRAM ROM

Crystal Castles Memory Map

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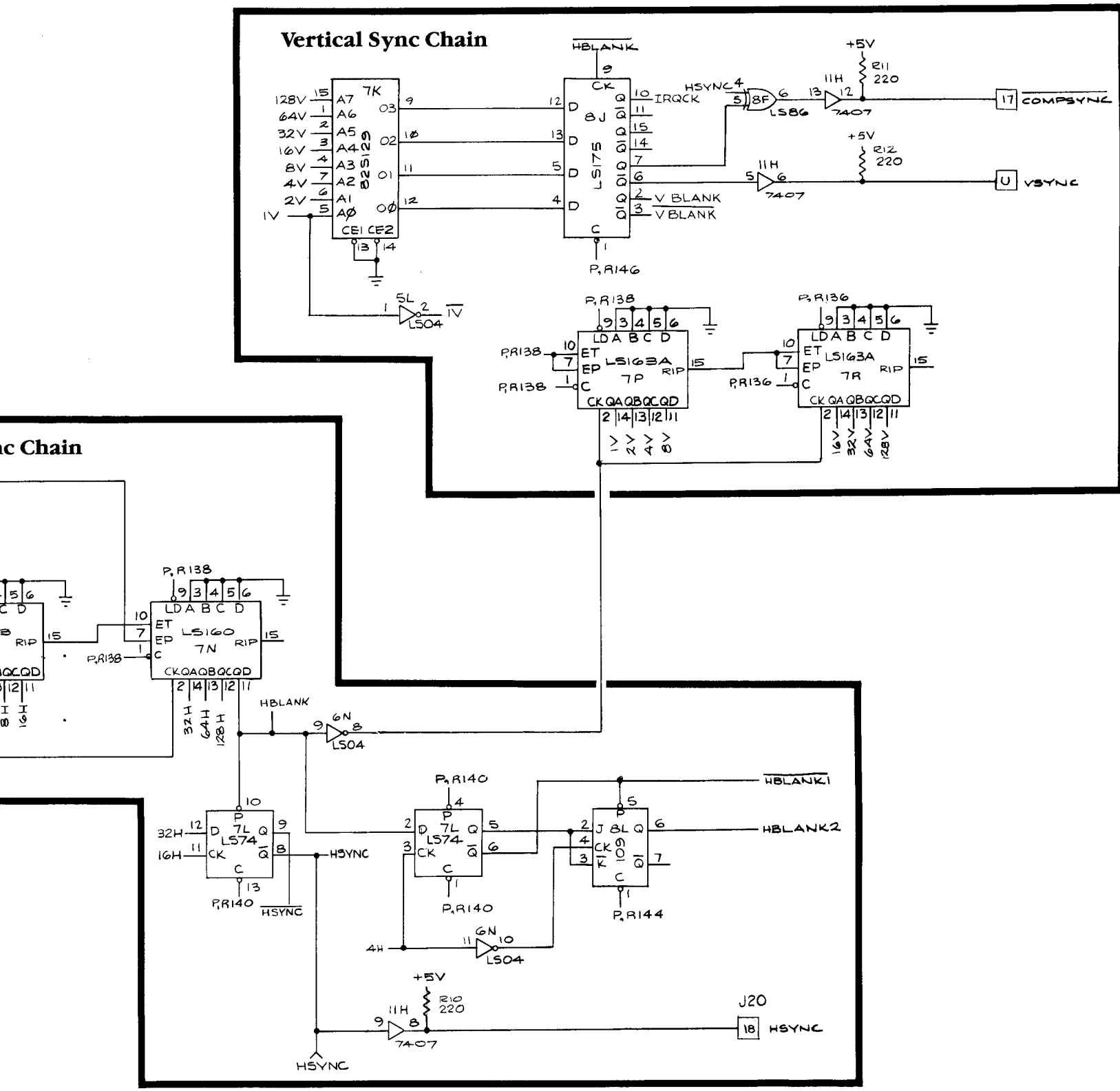
Crystal Castles Memory Map

HEXA-DECIMAL ADDRESS	ADDRESS BUS SIGNAL LINES A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	READ/ WRITE	DATA BUS SIGNAL LINES D7	D6	D5	D4	D3	D2	D1	D0
0000	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	W	X	X	X	X	X	X	X	X
0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	W	D	D	D	D	D	D	D	D
0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	R/W	D	D	D	D				
0003–0BFF	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D
0C00–7FFF	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D
8000–8DFF	1	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D
8E00–8EFF	1	0	0	0	1	1	1	0	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D
8F00–8FFF	1	0	0	0	1	1	1	1	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D
															0	0	R/W	D	D	D	D	D	D	D	D
															0	1	R/W	D	D	D	D	D	D	D	D
															1	0	R/W	D							
															1	1	R/W	D	D	D	D	D	D	D	D
9000–90FF	1	0	0	1	0	0	X	X	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D
9400–9403	1	0	0	1	0	1	0	X	X	X	X	X	X	X	A	A	R								
4600	1	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	R								
																	R								D
																	R							D	
																	R						D		
																	R					D			
																	R				D				
																	R			D					
																	R		D						
																	R	D							
9800–980F	1	0	0	1	1	0	0	X	X	X	X	X	A	A	A	A	R/W	D	D	D	D	D	D	D	D
9A00–9A0F	1	0	0	1	1	0	1	X	X	X	X	X	A	A	A	A	R/W	D	D	D	D	D	D	D	D
9A08																							D	D	D
																						D			
																					D				
																				D					
9C00	1	0	0	1	1	1	0	0	0	X	X	X	X	X	X	X	W								
9C80	1	0	0	1	1	1	0	0	1	X	X	X	X	X	X	X	W	D	D	D	D	D	D	D	D
9D00	1	0	0	1	1	1	0	1	0	X	X	X	X	X	X	X	W	D	D	D	D	D	D	D	D
9D80	1	0	0	1	1	1	0	1	1	X	X	X	X	X	X	X	W								
9E00	1	0	0	1	1	1	1	0	0	X	X	X	X	X	X	X	W								
	1	0	0	1	1	1	1	0	1	X	X	X	X	A	A	A	W								D
9E80														0	0	0	W								D
9E81														0	0	1	W								D
9E82														0	1	0	W								D
9E83														0	1	1	W								D
9E84														1	0	0	W								D
9E85														1	0	1	W								D
9E86														1	1	0	W								D
9E87														1	1	1	W								D
	1	0	0	1	1	1	1	1	0	X	X	X	X	A	A	A	W					D			
9F00														0	0	0	W					D			
9F01														0	0	1	W					D			
9F02														0	1	0	W					D			
9F03														0	1	1	W					D			
9F04														1	0	0	W					D			
9F05														1	0	1	W					D			
9F06														1	1	0	W					D			
9F07														1	1	1	W					D			
9F80–9FBF	1	0	0	1	1	1	1	1	1	X	A	A	A	A	A	A	W	D	D	D	D	D	D	D	D
A000–FFFF	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D



Crystal Castles PCB Schematic Diagram

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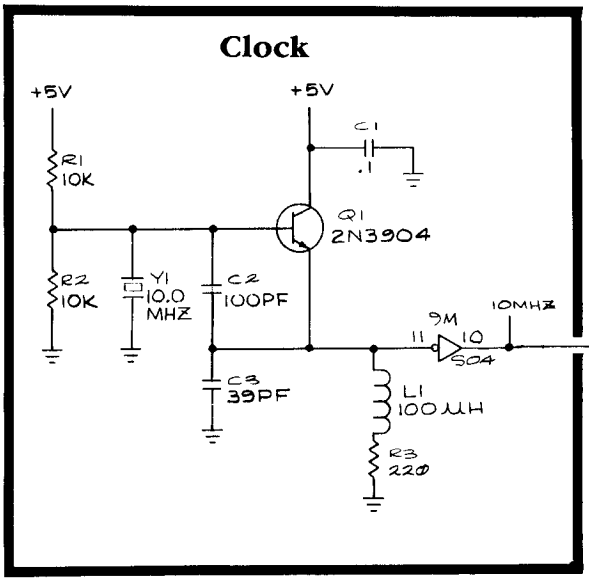
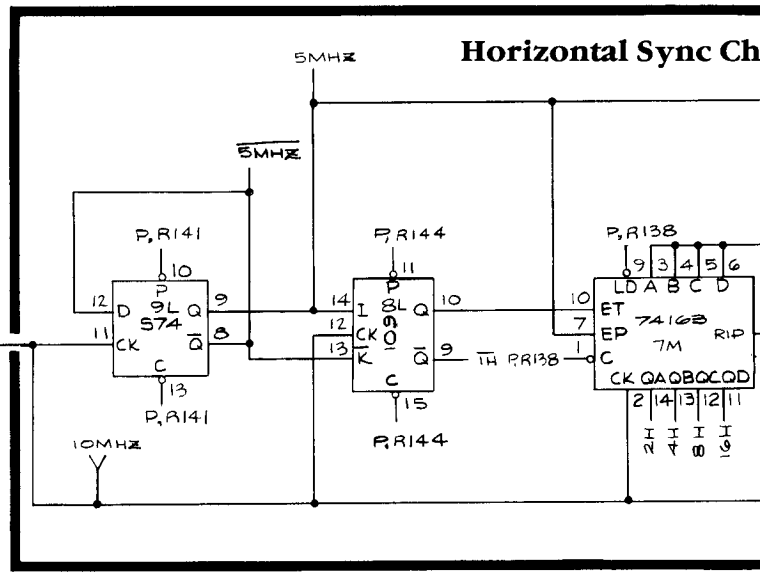
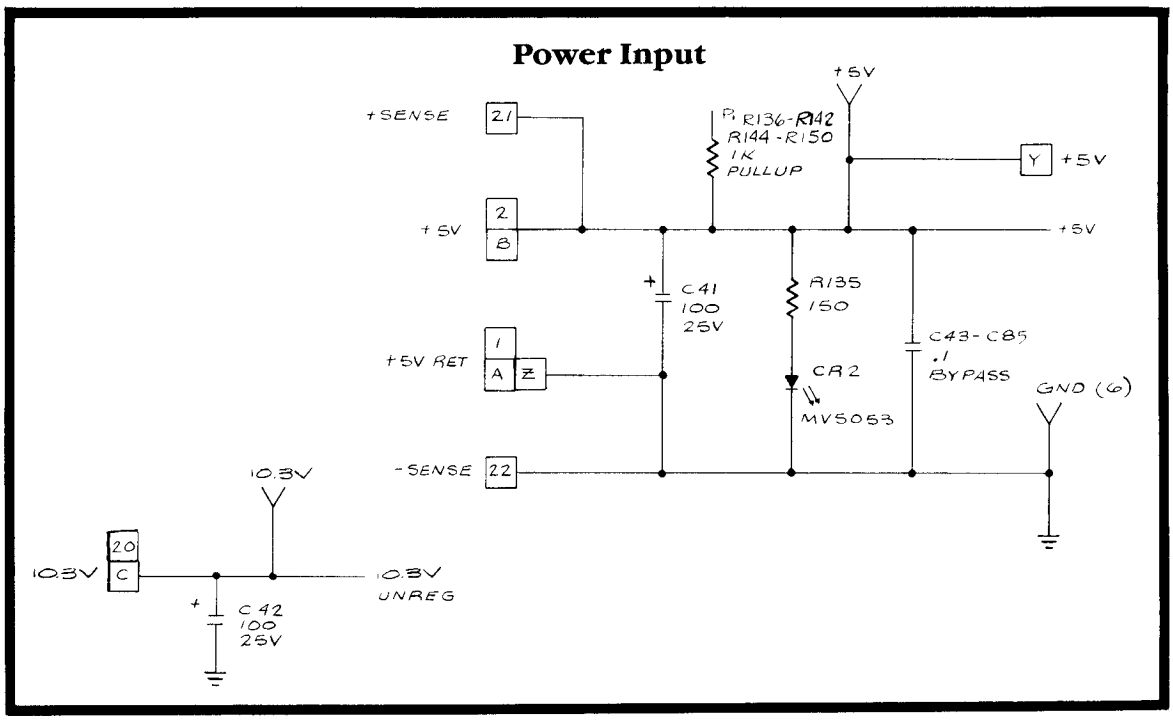
Connector Symbols

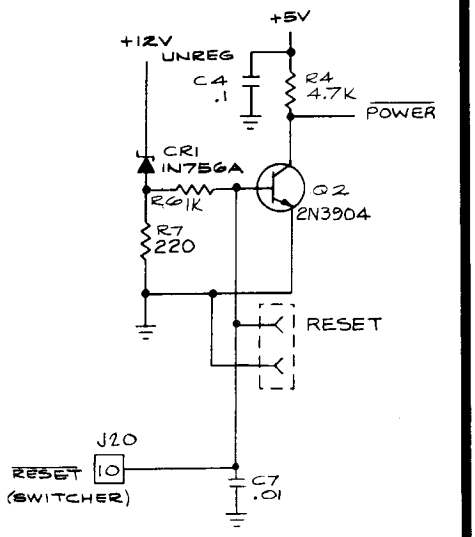
1. ▭ DENOTES J20 CONNECTOR.
2. ⬭ DENOTES J19 CONNECTOR.
3. ○ DENOTES TEST CONNECTOR.



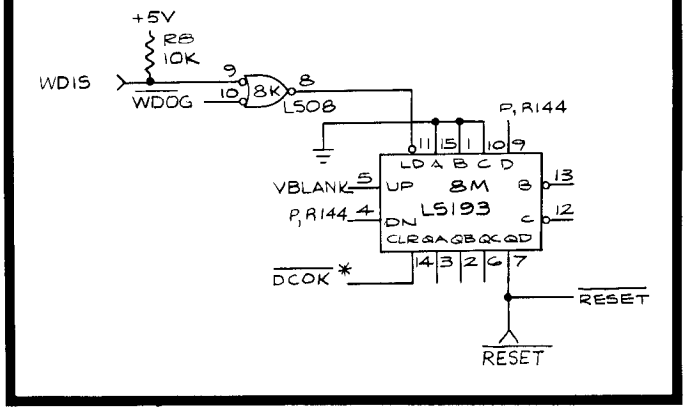




Power-On Reset



Watchdog



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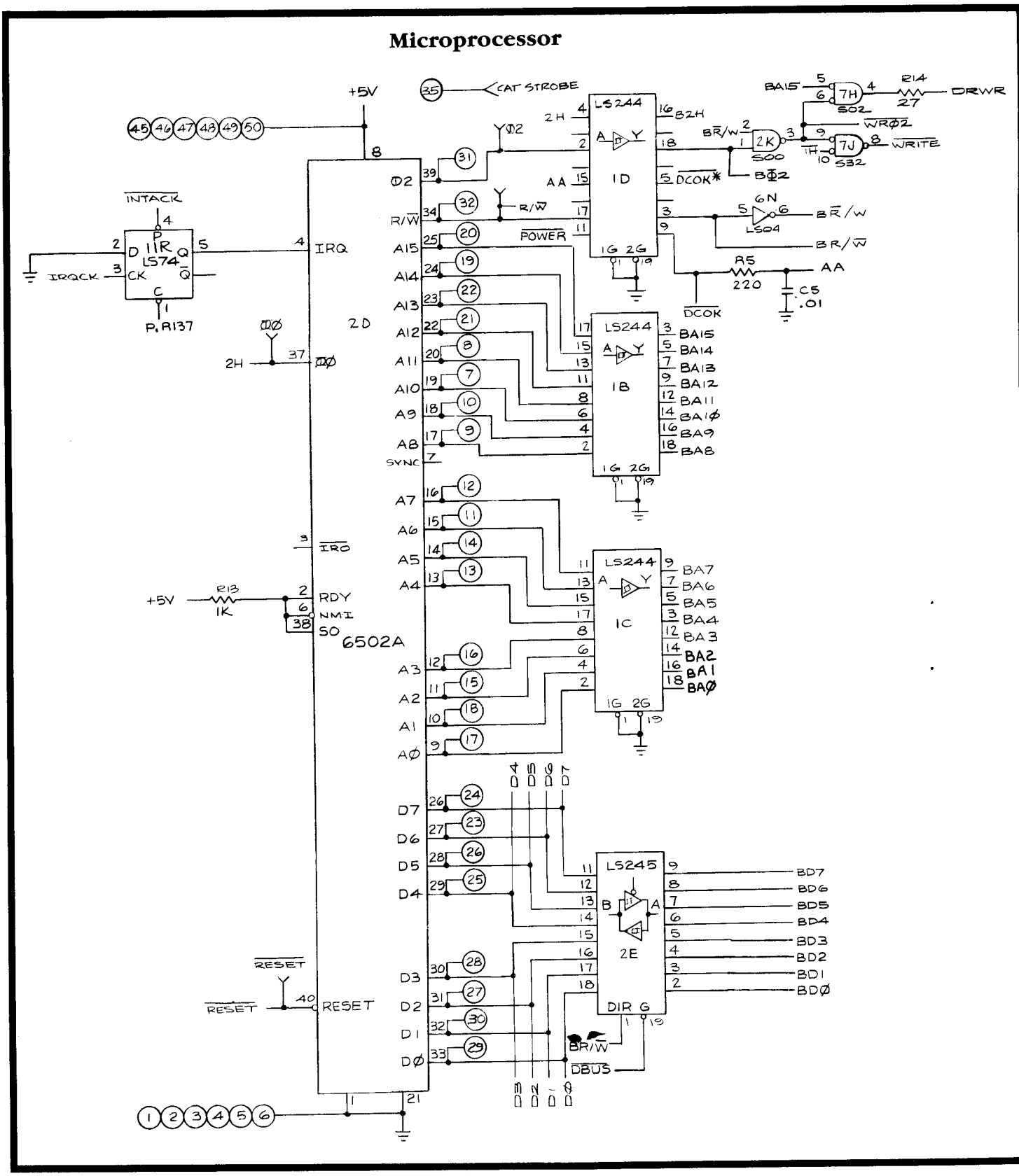
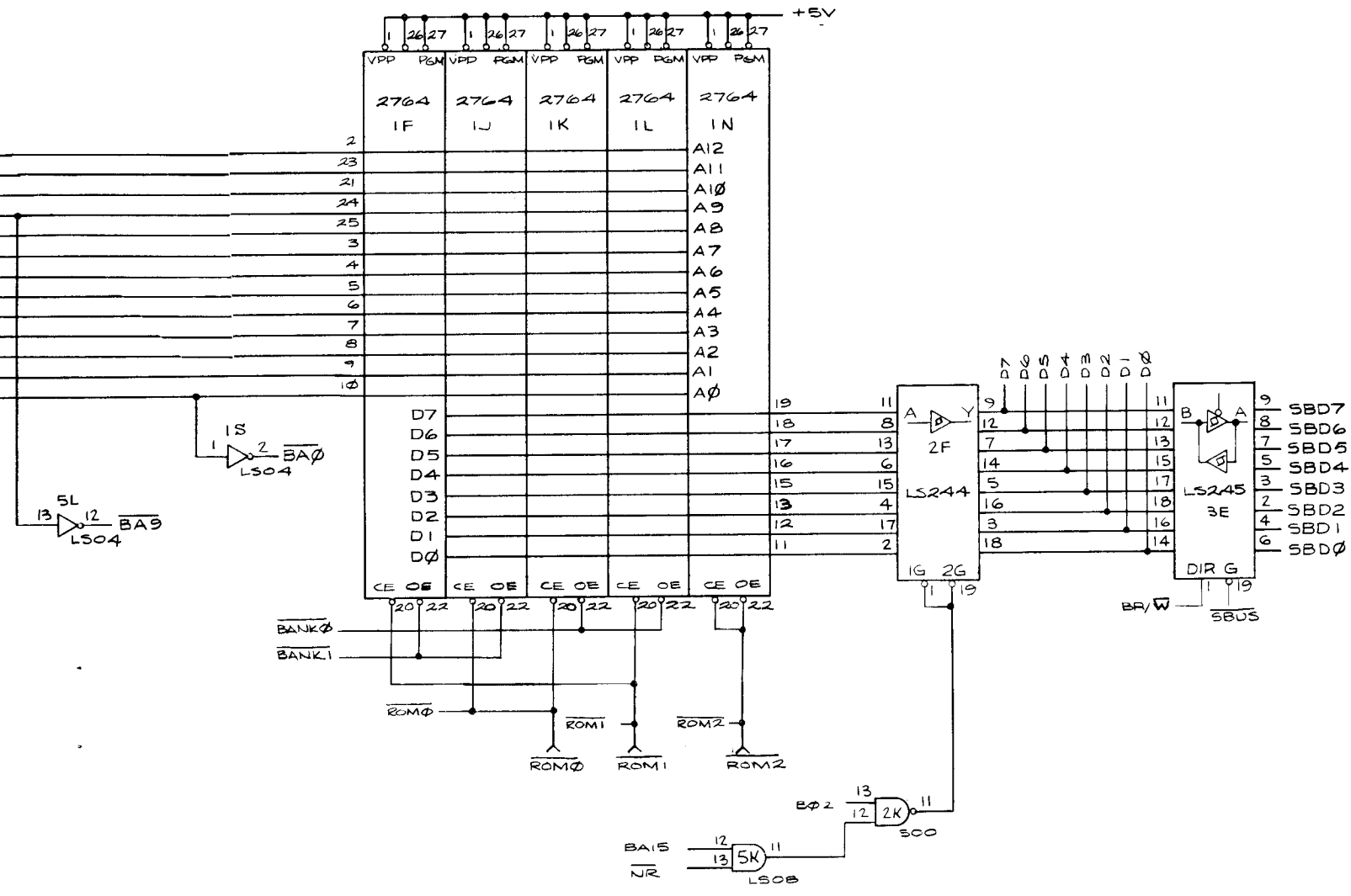
Microprocessor



Program Memory



Crystal Castles PCB Schematic Diagram

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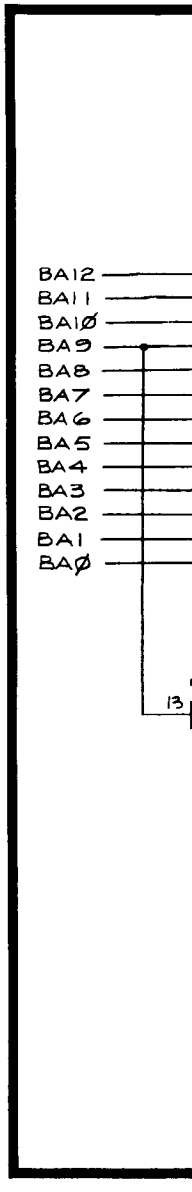
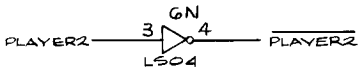
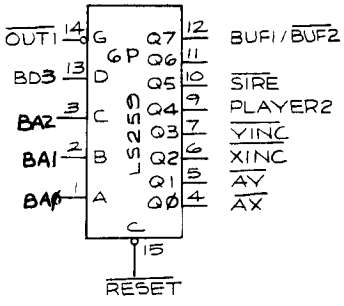
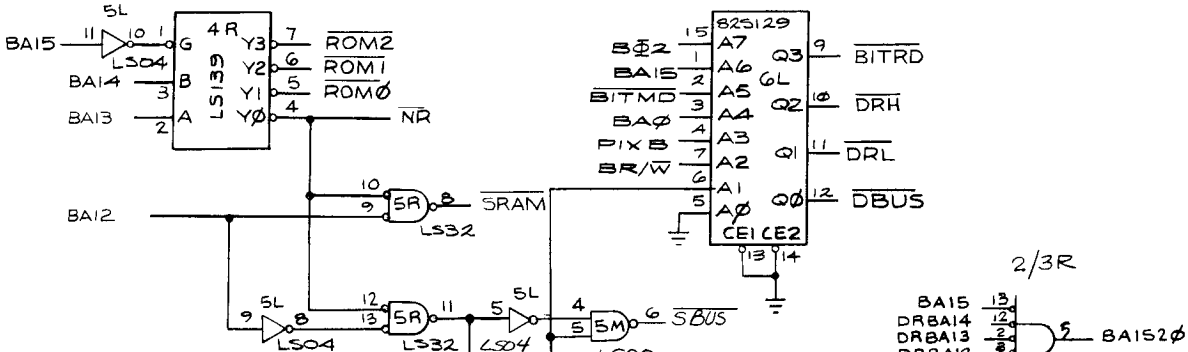
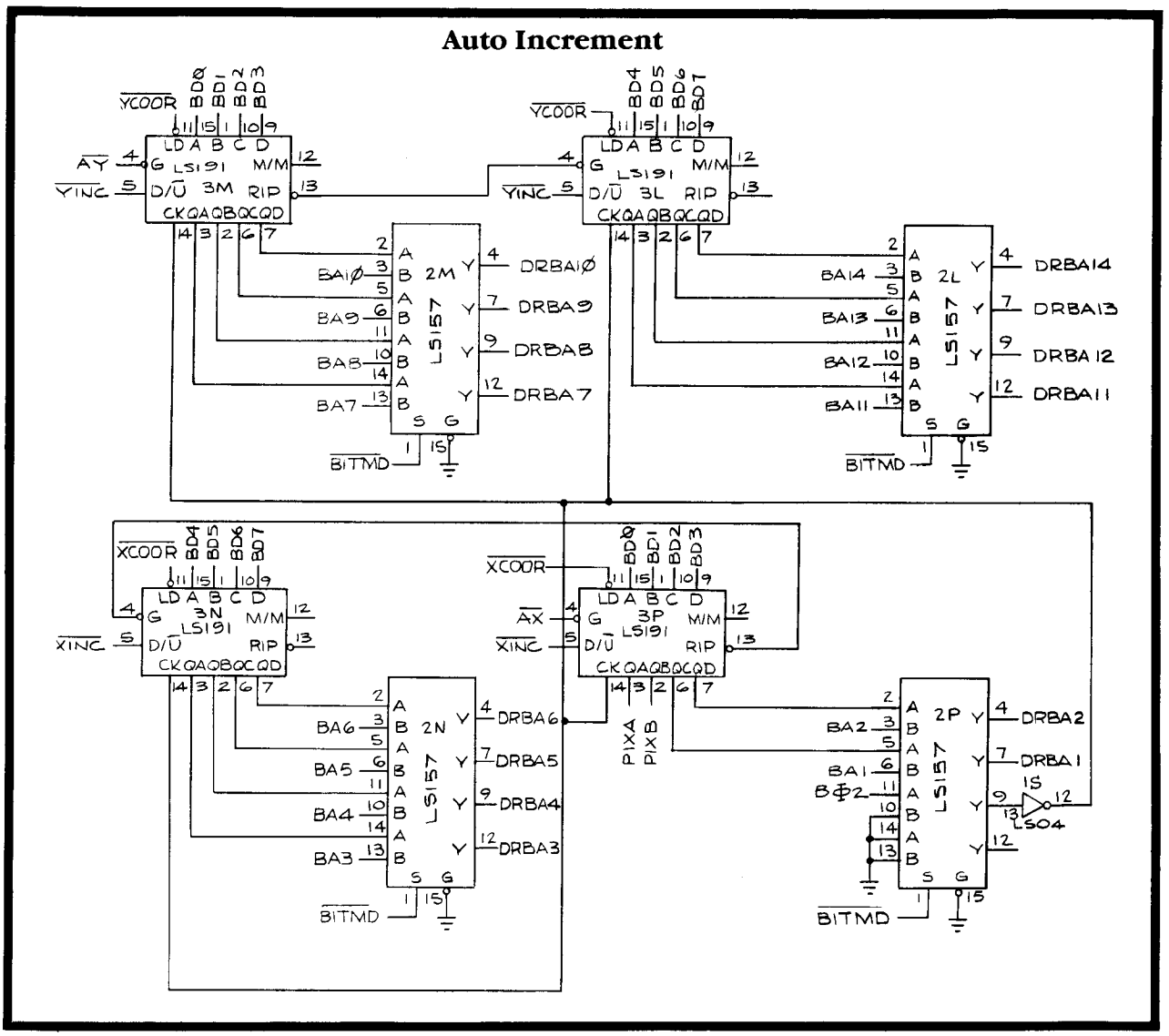


Address Decoders









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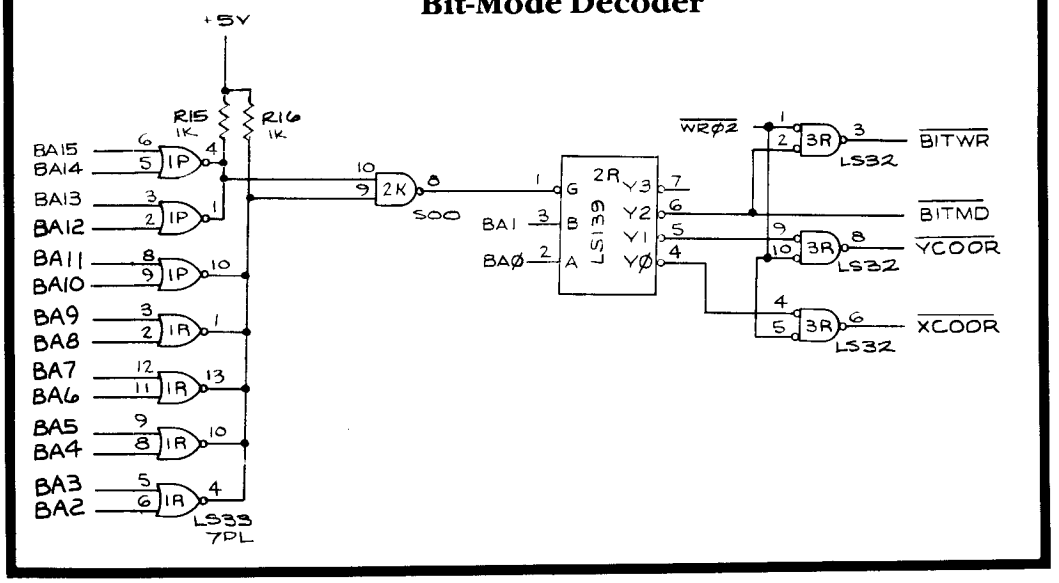
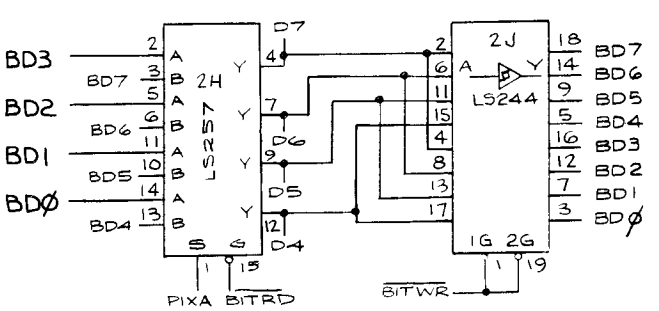
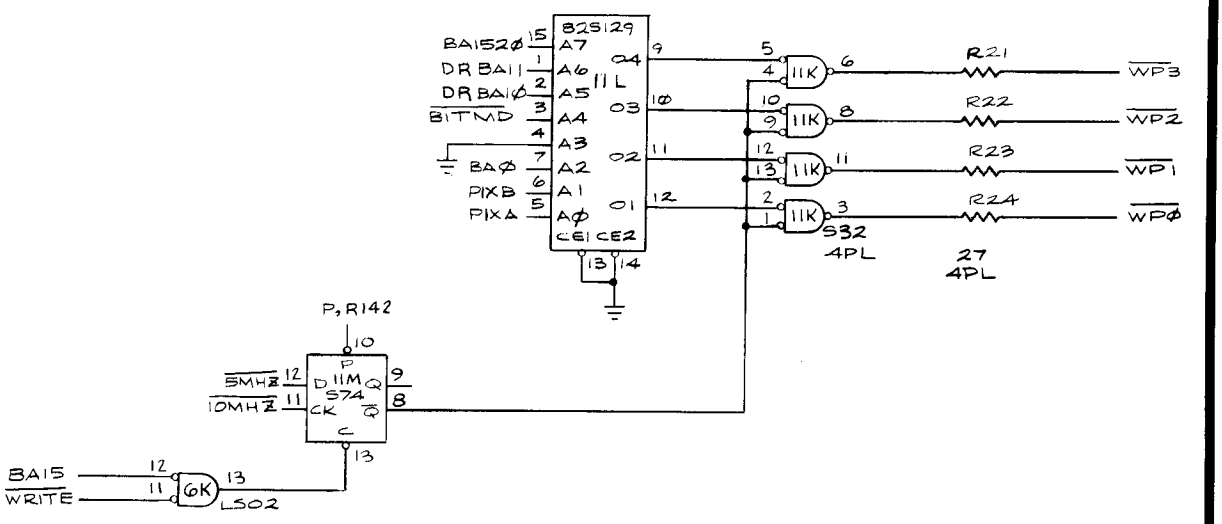
Bit-Mode Decoder



Bit-Mode Read/Write



Dynamic RAM Write Protection



Crystal Castles PCB Schematic Diagram

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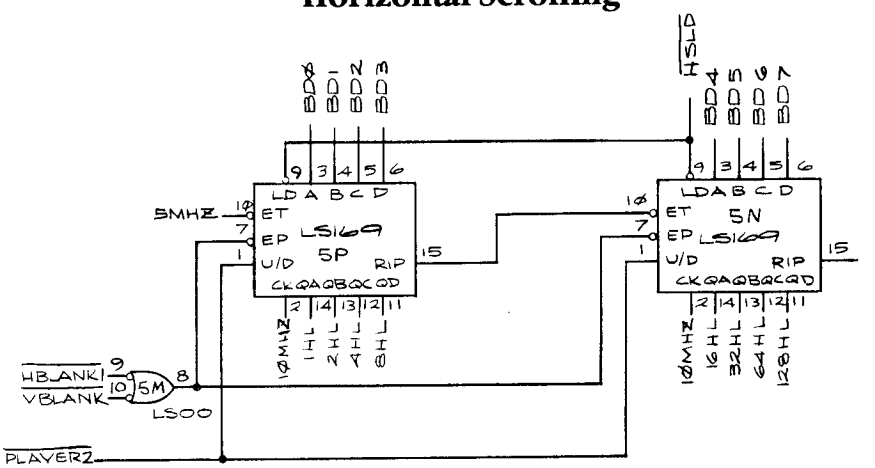
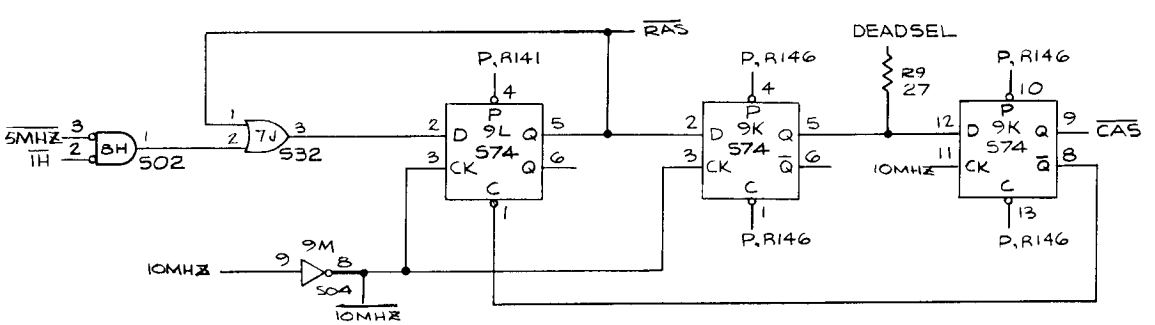
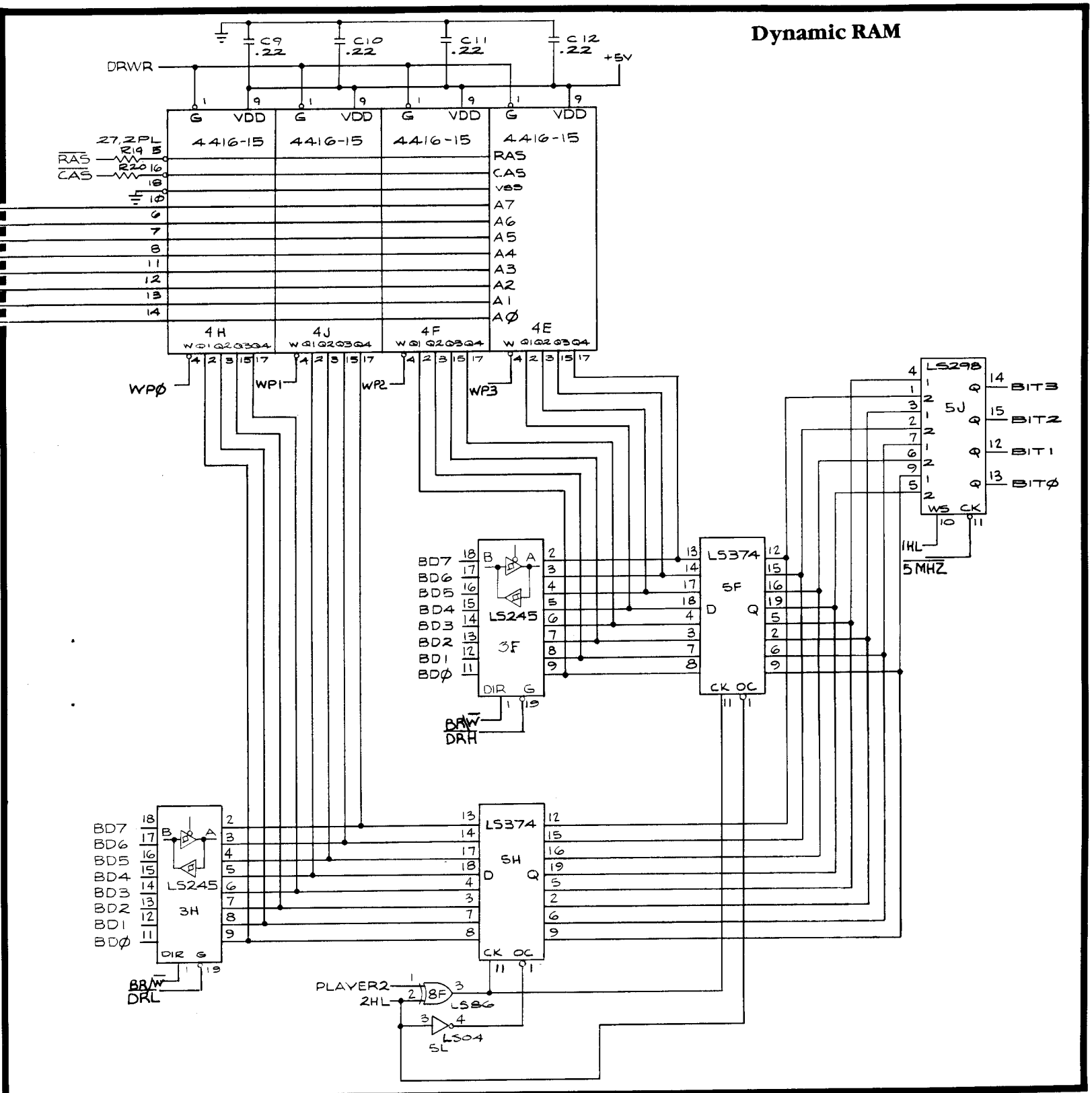
Horizontal Scrolling



Dynamic RAM Control



Dynamic RAM



Crystal Castles PCB Schematic Diagram

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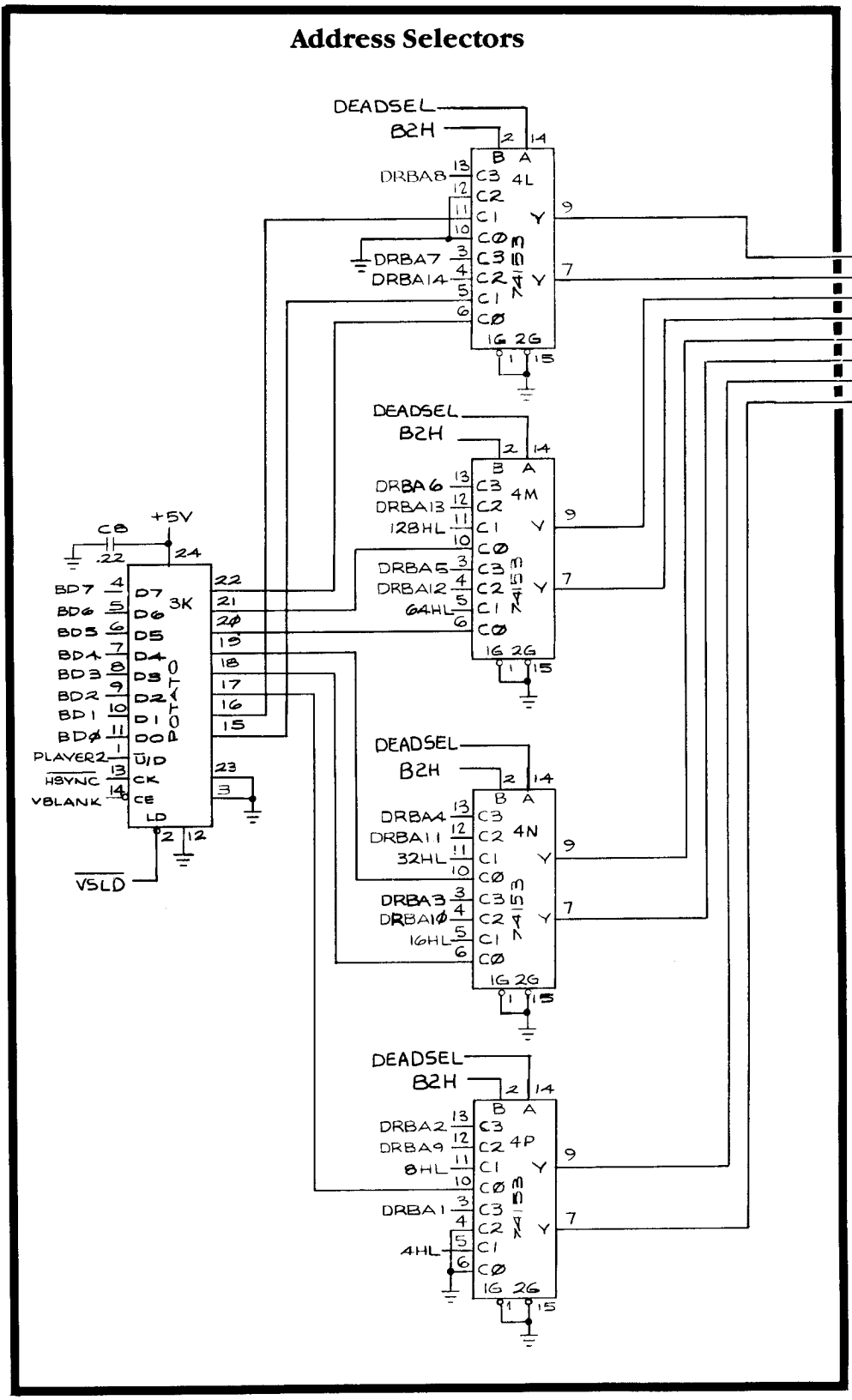
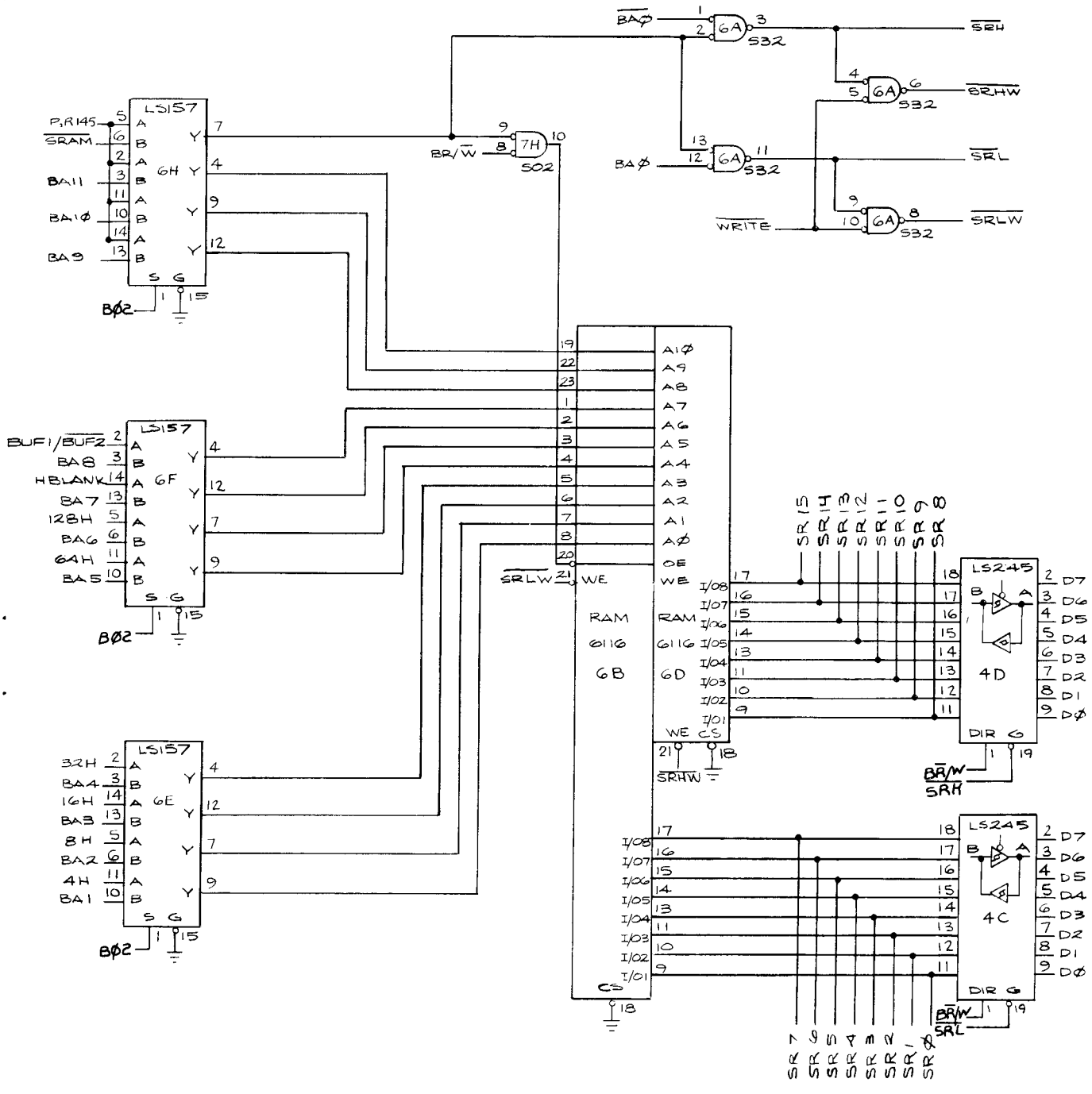
Address Selectors



Working RAM and Motion-Object RAM



Crystal Castles PCB Schematic Diagram

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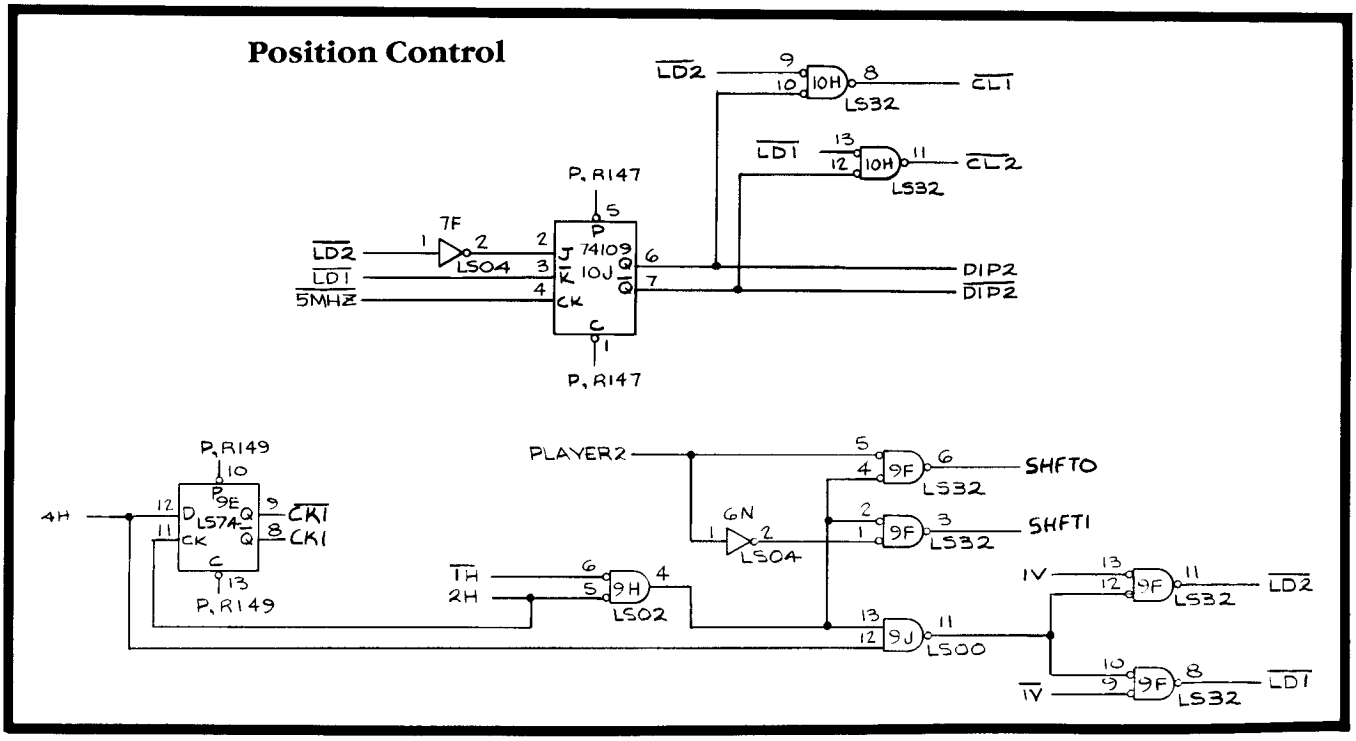
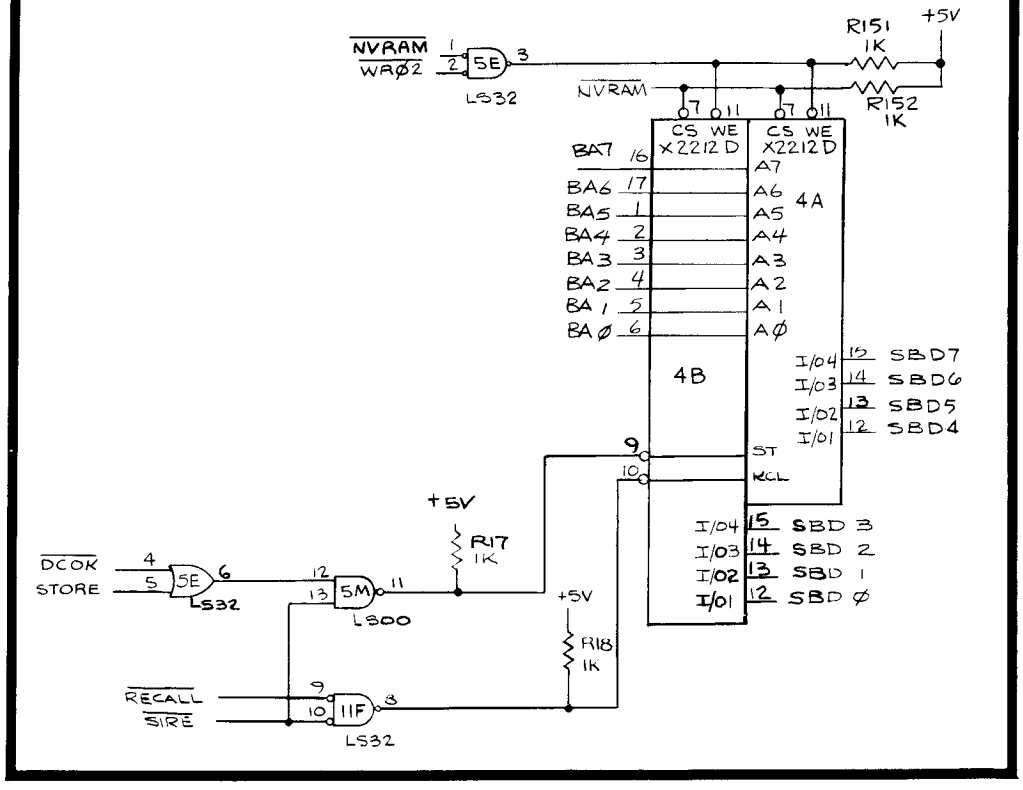
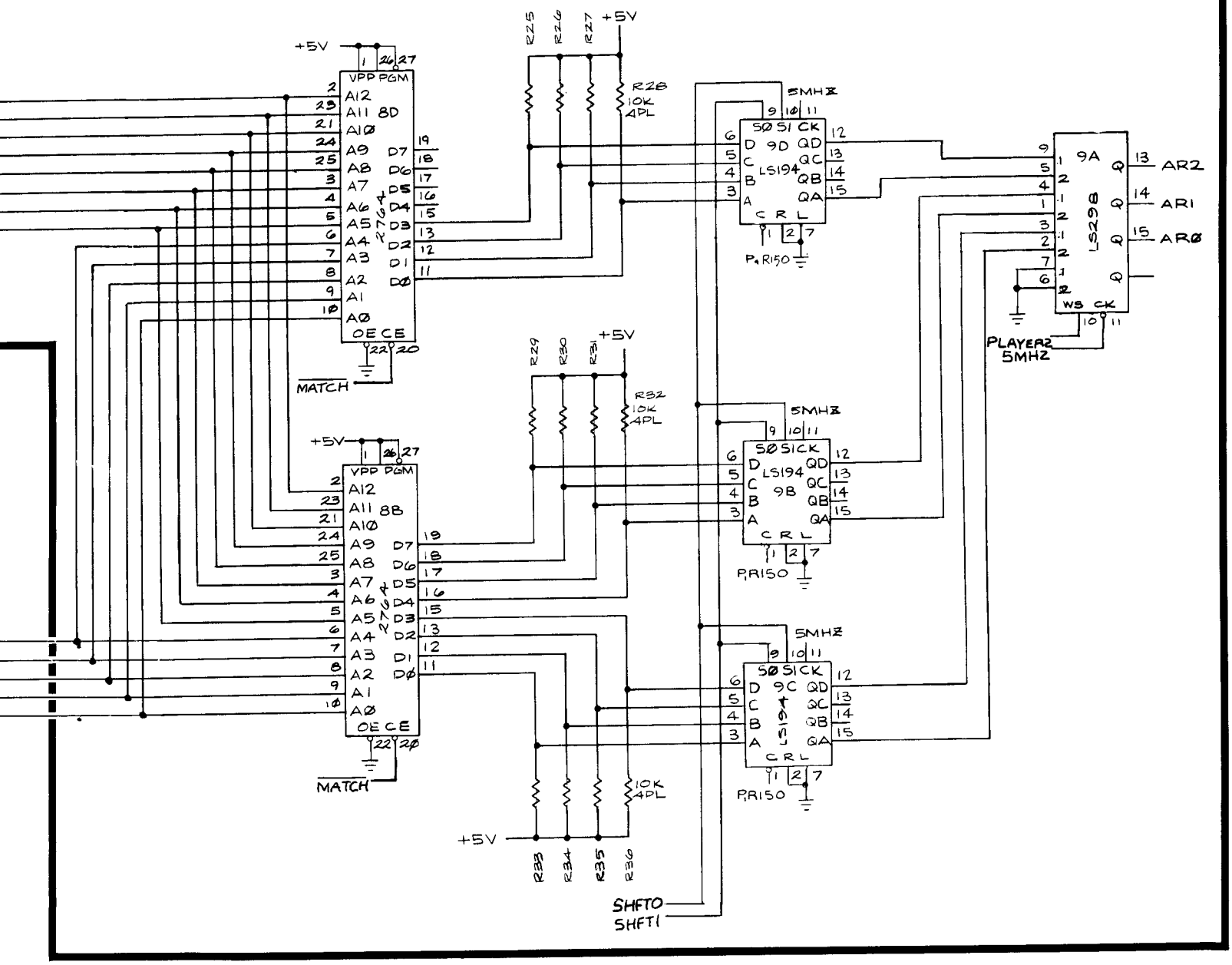
Position Control



Non-Volatile RAM



Motion-Object Picture ROM



Crystal Castles PCB Schematic Diagram

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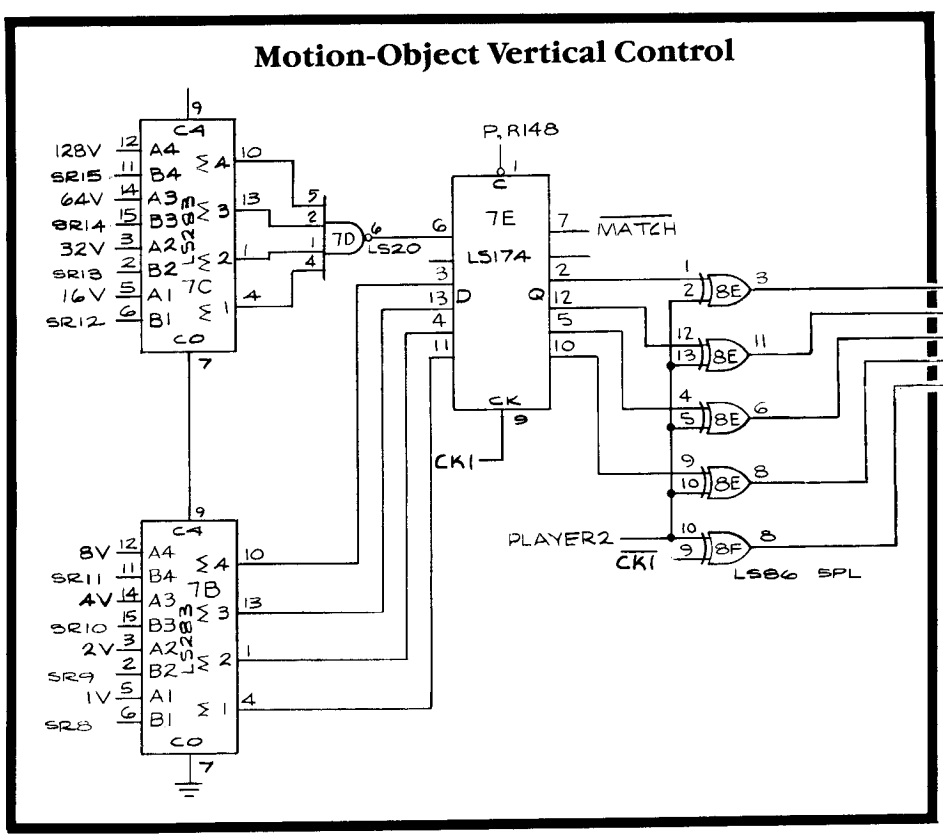
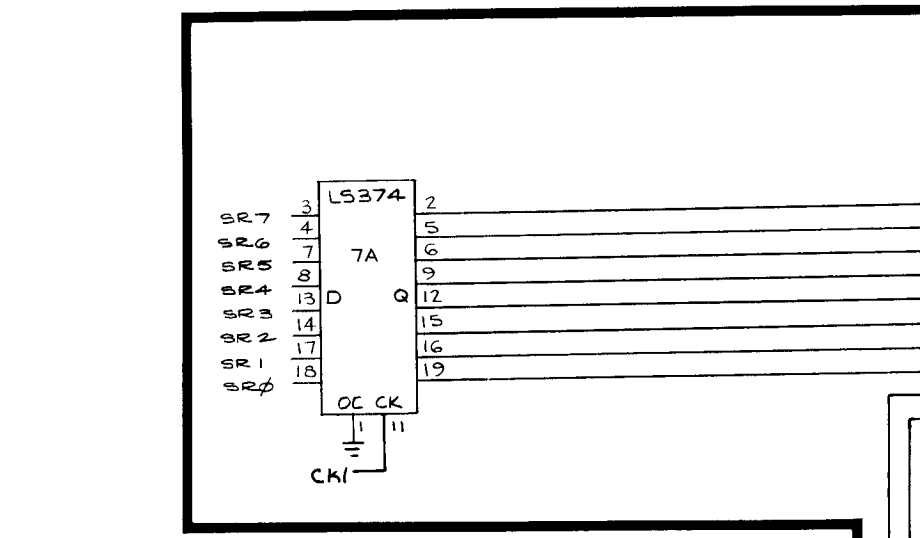
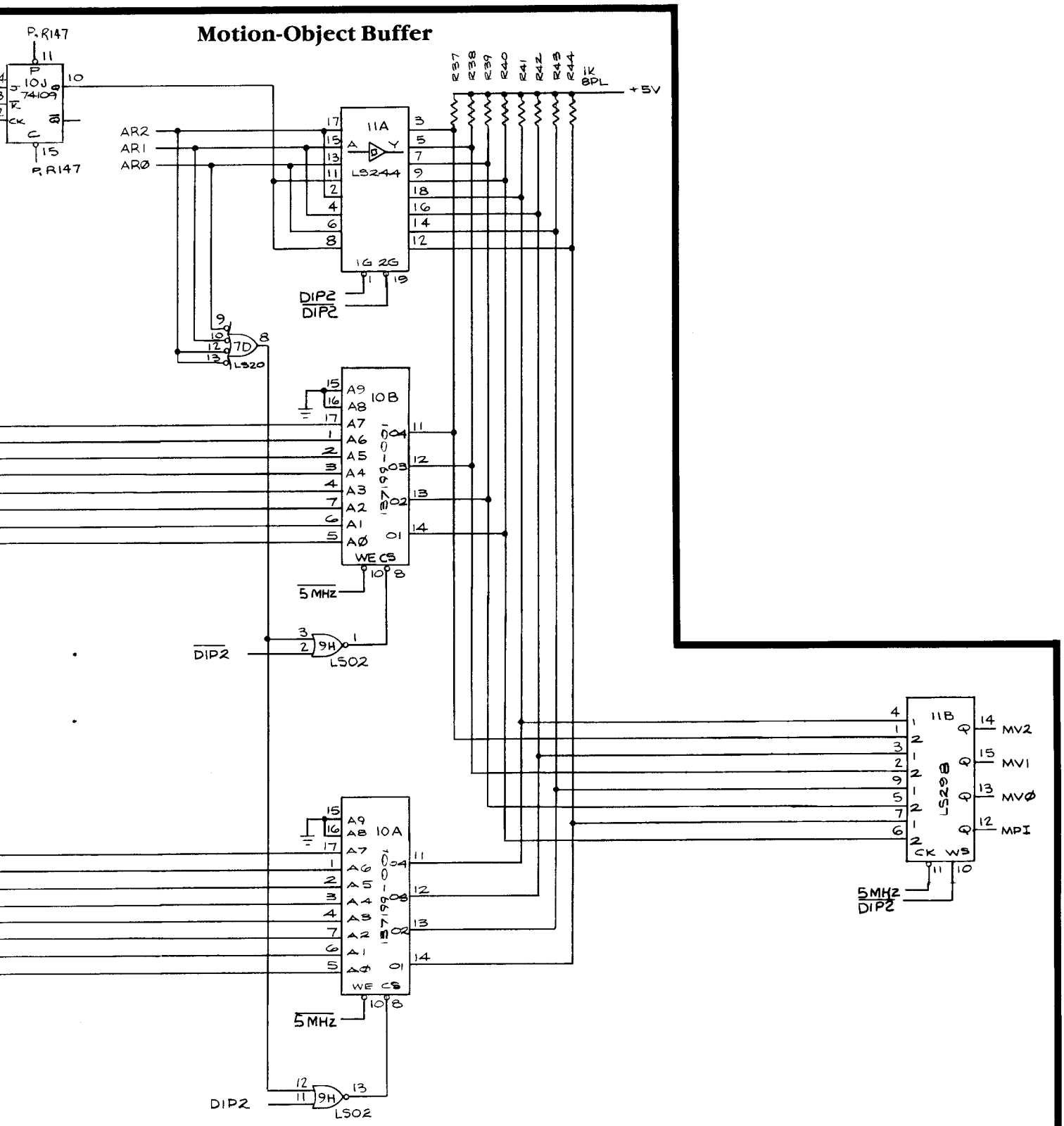

Motion-Object Vertical Control
128V
SR15
64V
SR14
32V
SR13
16V
SR12
8V
SR11
4V
SR10
2V
SR9
1V
SR8
7C
7B
LS283
7D
LS20
7E
LS174
P.R148
MATCH
CK1
PLAYER2
8E
8F
LS86 SPL


LS374
7A
SR7
SR6
SR5
SR4
SR3
SR2
SR1
SR0
D
Q
OC
CK
CK1



Crystal Castles PCB Schematic Diagram

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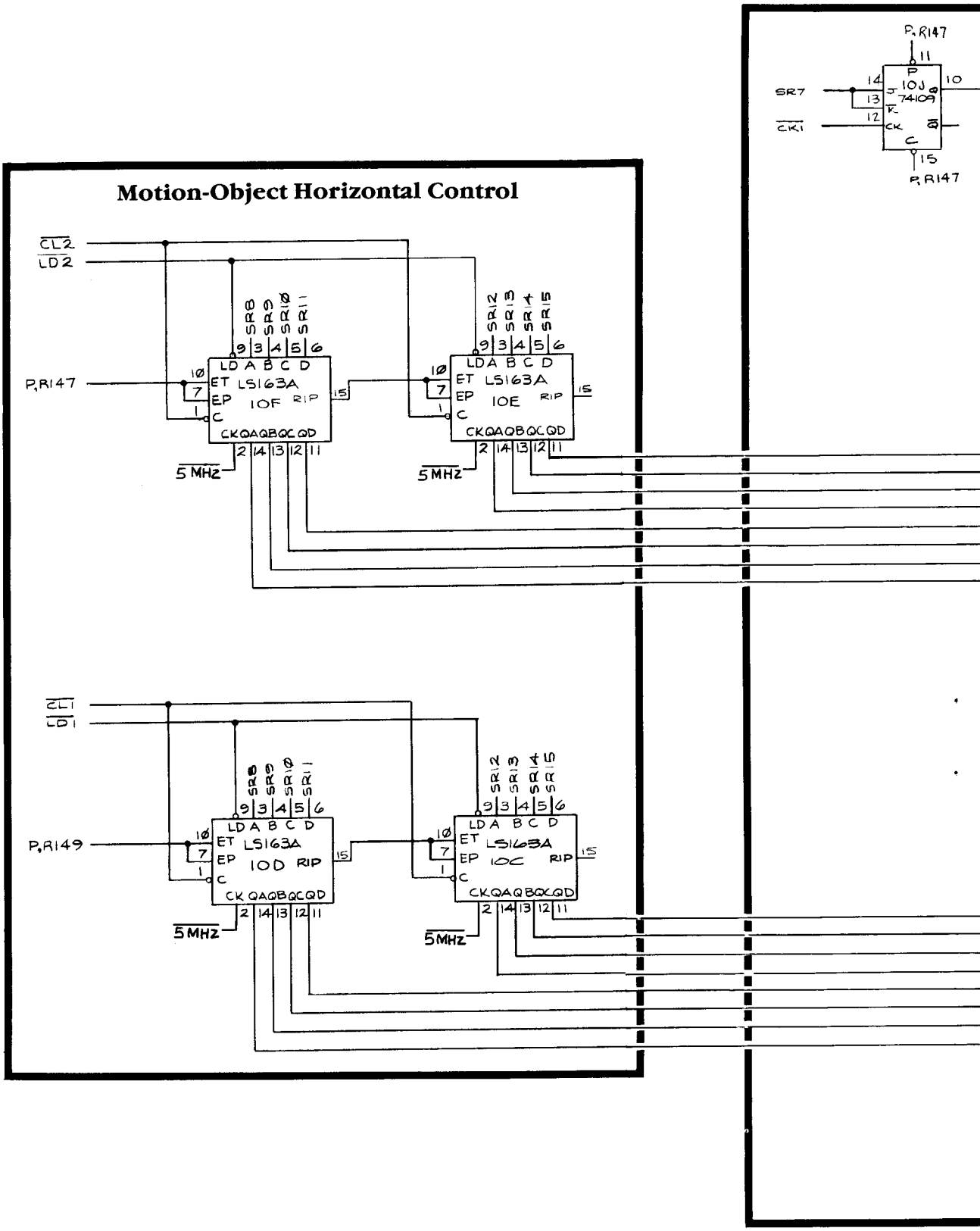
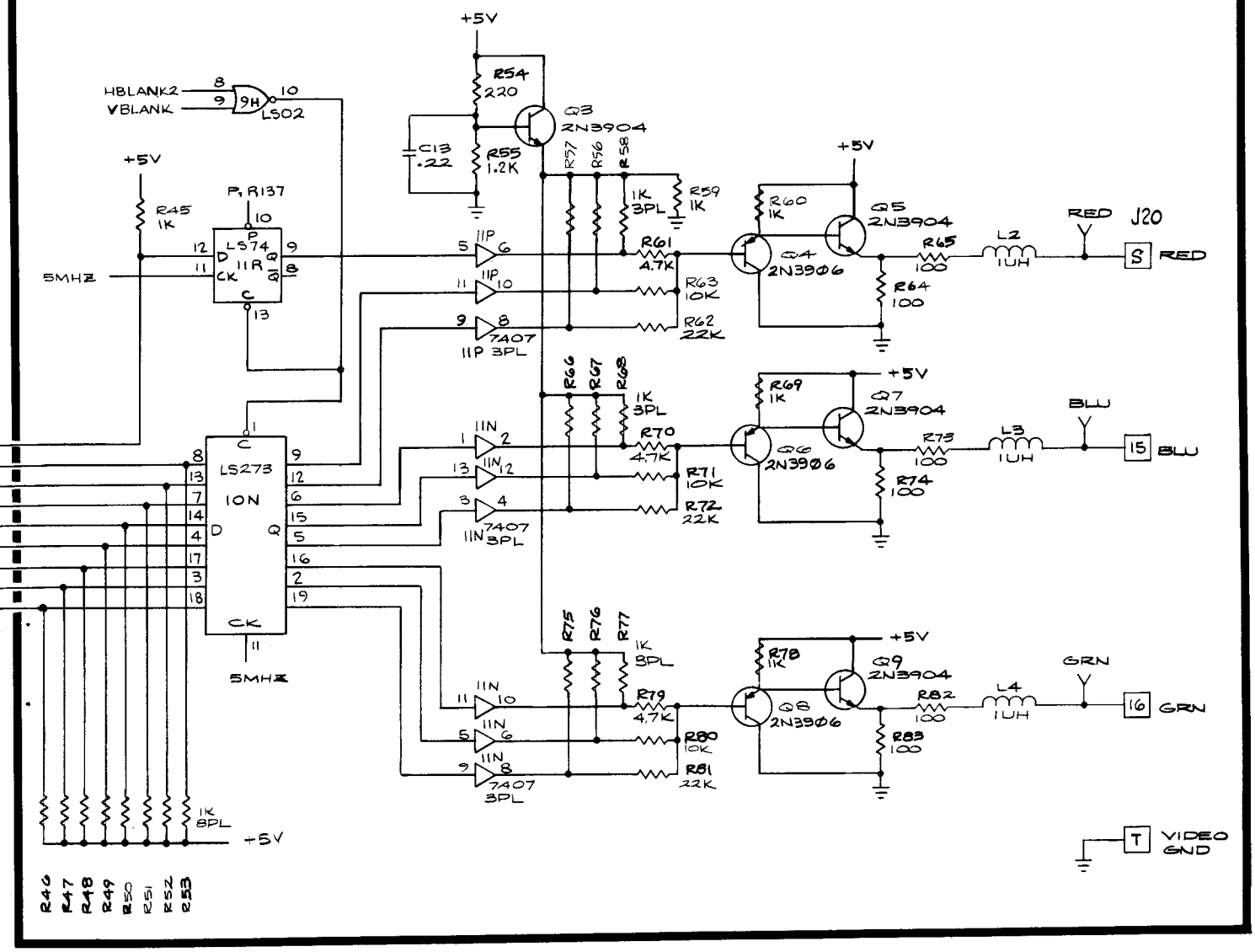
1st printing


Motion-Object Horizontal Control
P,R147
11
P
10J
74109
14
J
13
K
12
CK
C
15
10
SR7
CK1
P,R147
CL2
LD2
SR8
SR9
SR10
SR11
SR12
SR13
SR14
SR15
9 3 4 5 6
LD A B C D
10
7
1
ET LS163A
EP 10F RIP
C
CK QA QB QC QD
15
2 14 13 12 11
5 MHz
P,R147
10E
P,R149
CL1
LD1
10D
10C

Color Output



Crystal Castles PCB Schematic Diagram

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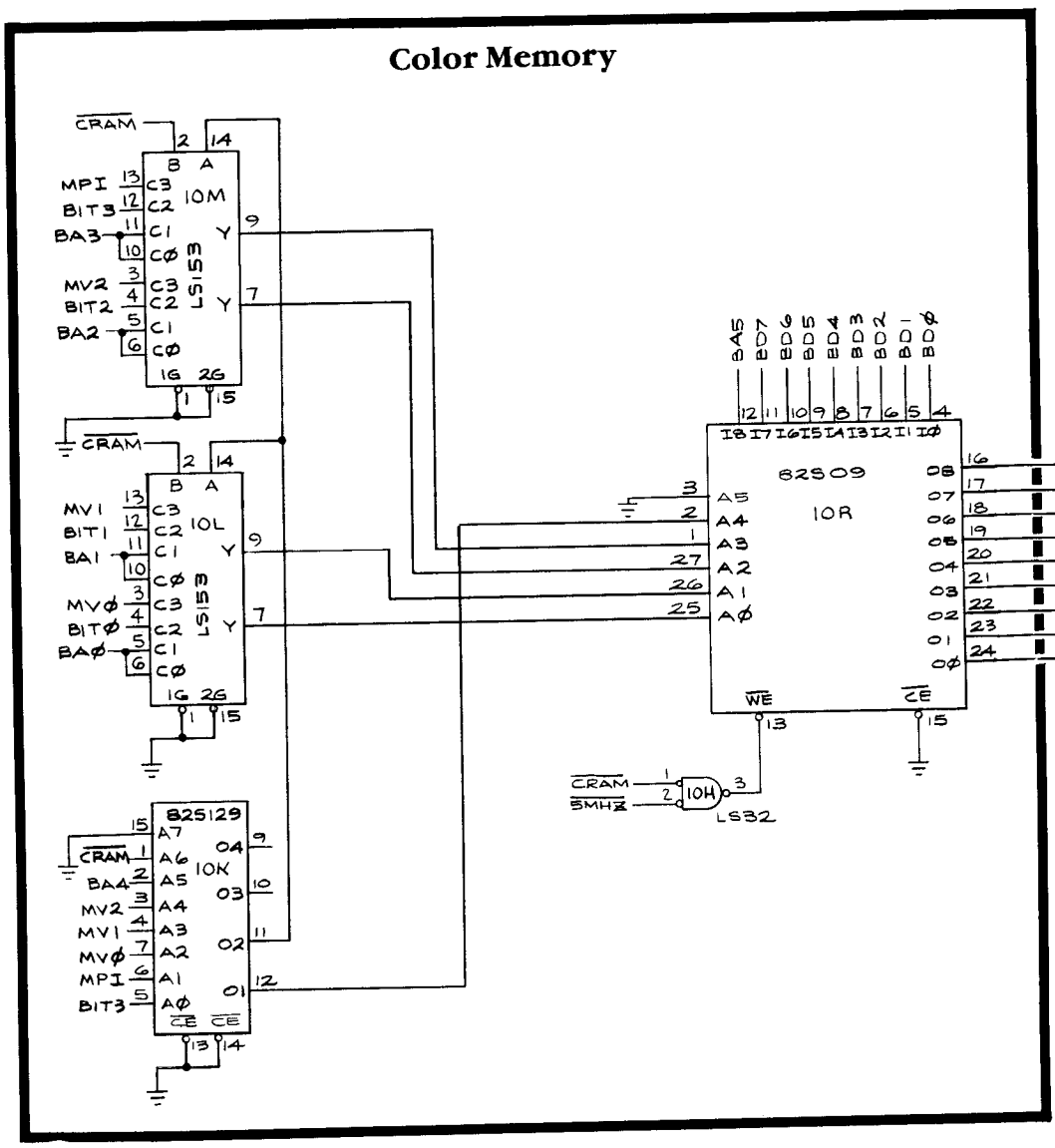
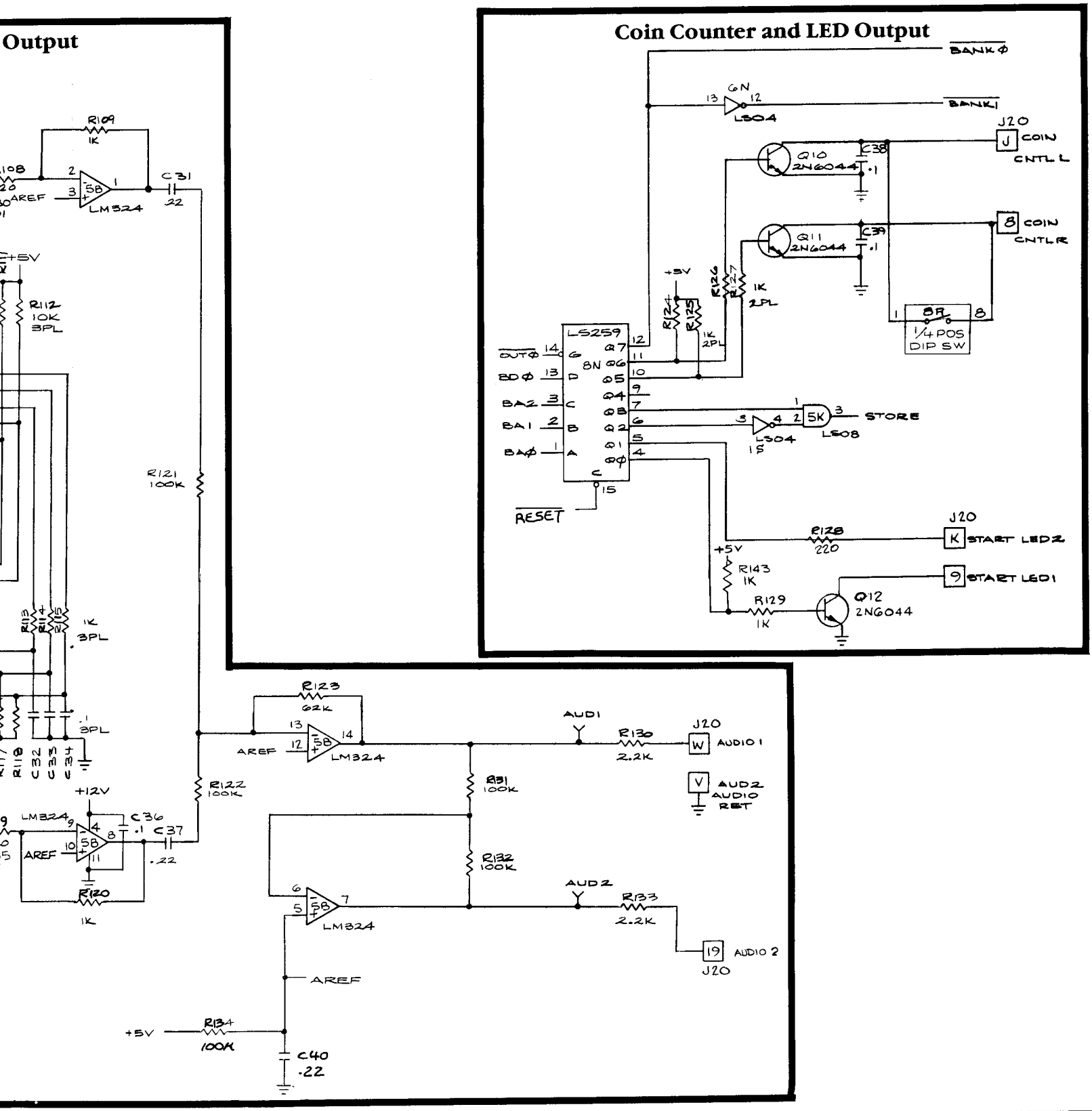
1st printing


Color Memory
CRAM
MPI
BIT3
BA3
MV2
BIT2
BA2
10M
LS153
MV1
BIT1
BA1
MVØ
BITØ
BAØ
10L
825129
BA4
10K
825109
10R
WE
CE
5MHZ
10H
LS32



Crystal Castles PCB Schematic Diagram

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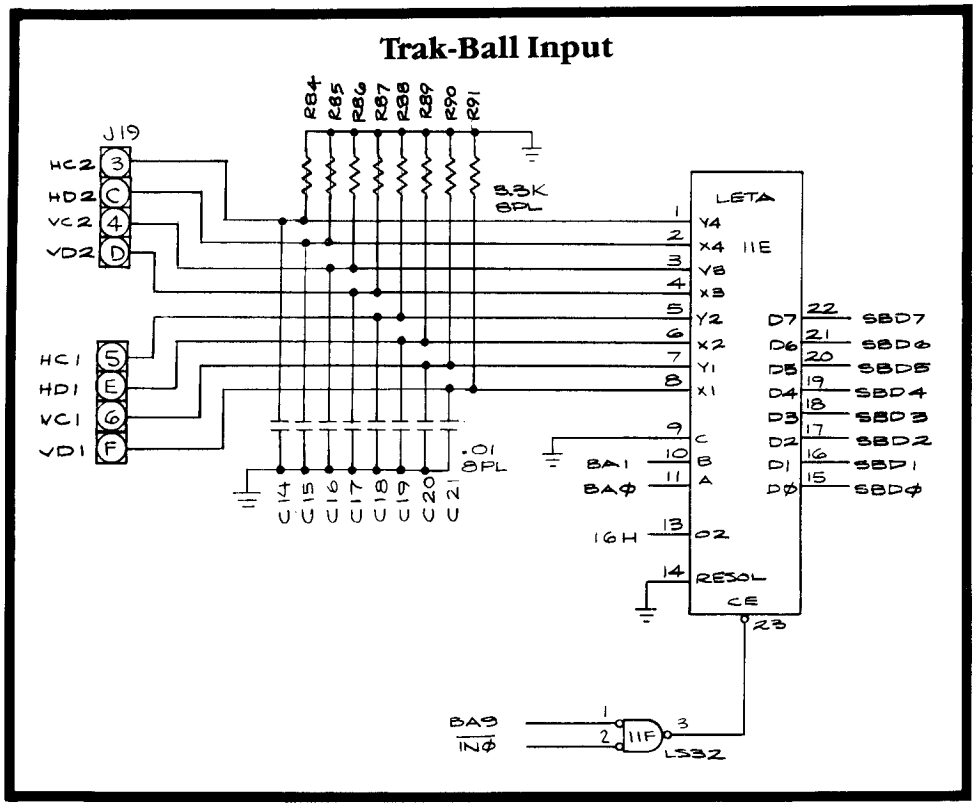
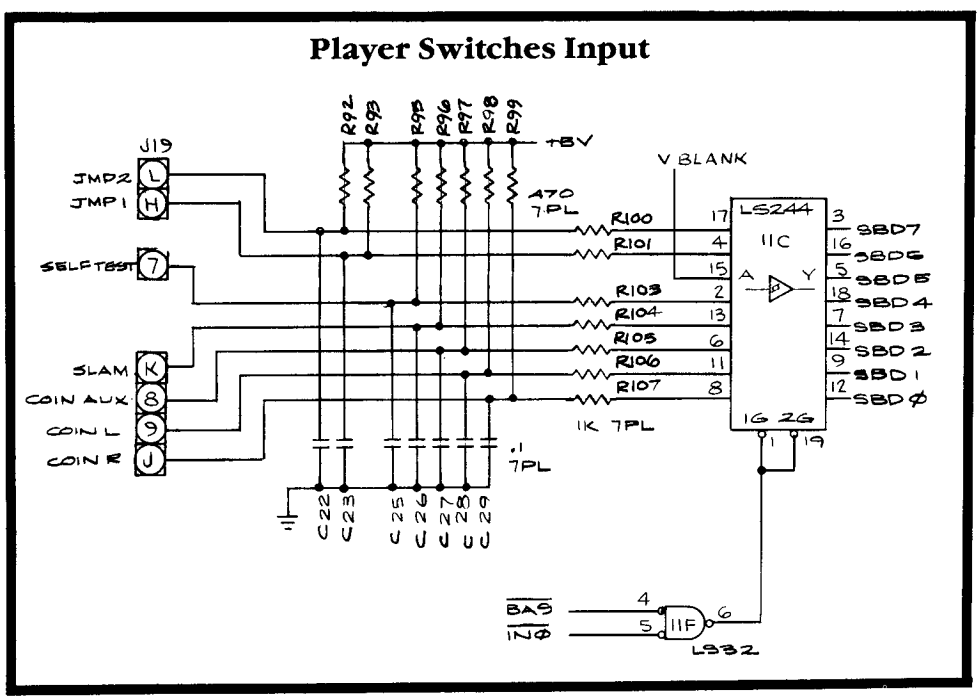
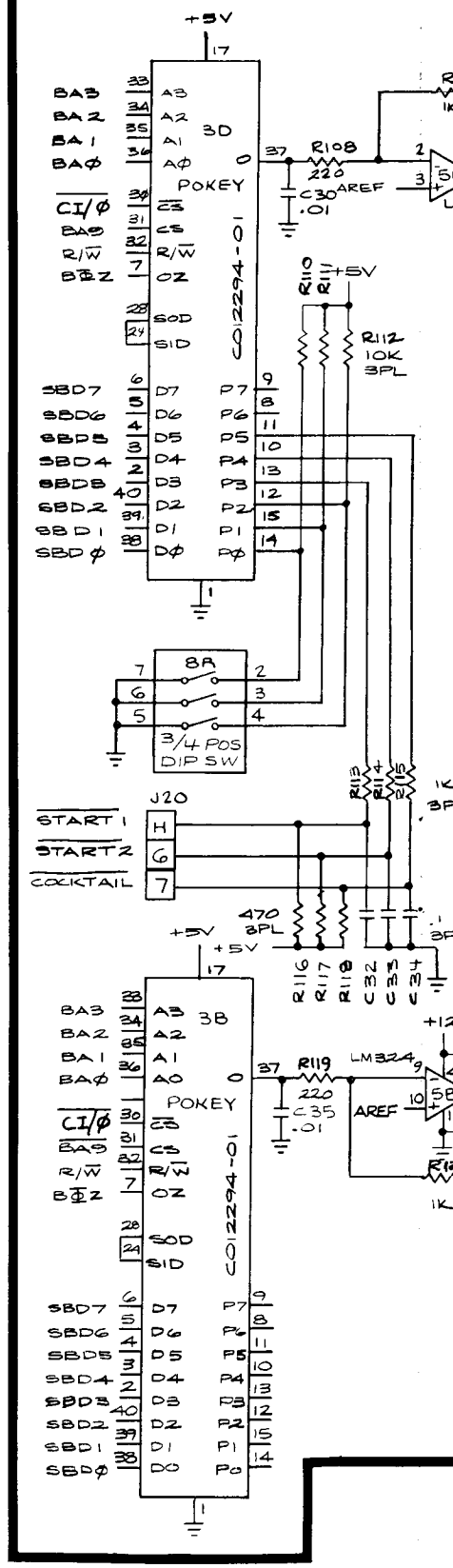
Trak-Ball Input

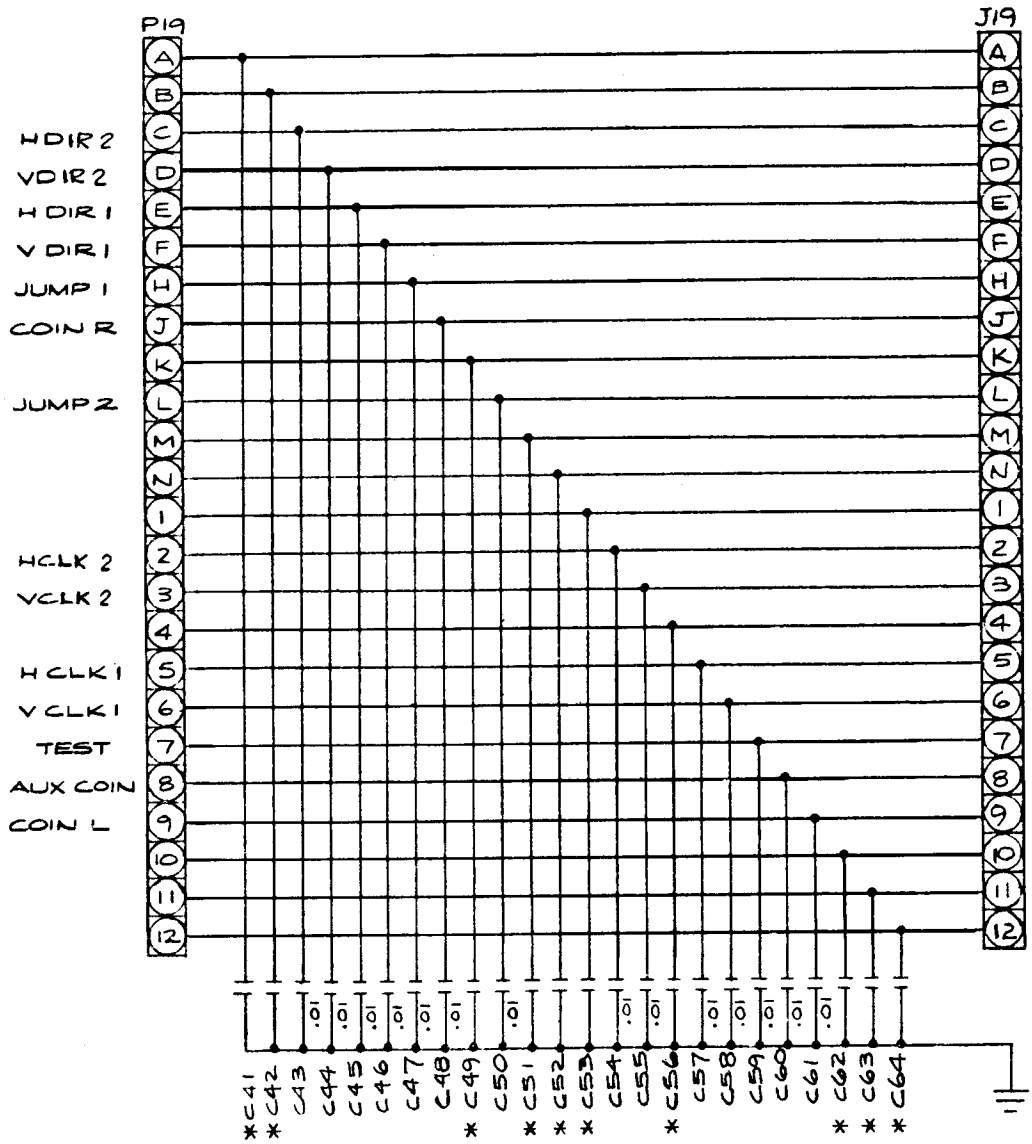


Player Switches Input



Audio Output





NOTES:

1. * DENOTES NOT LOADED CAPACITOR.

Crystal Castles EMI Shield PCB

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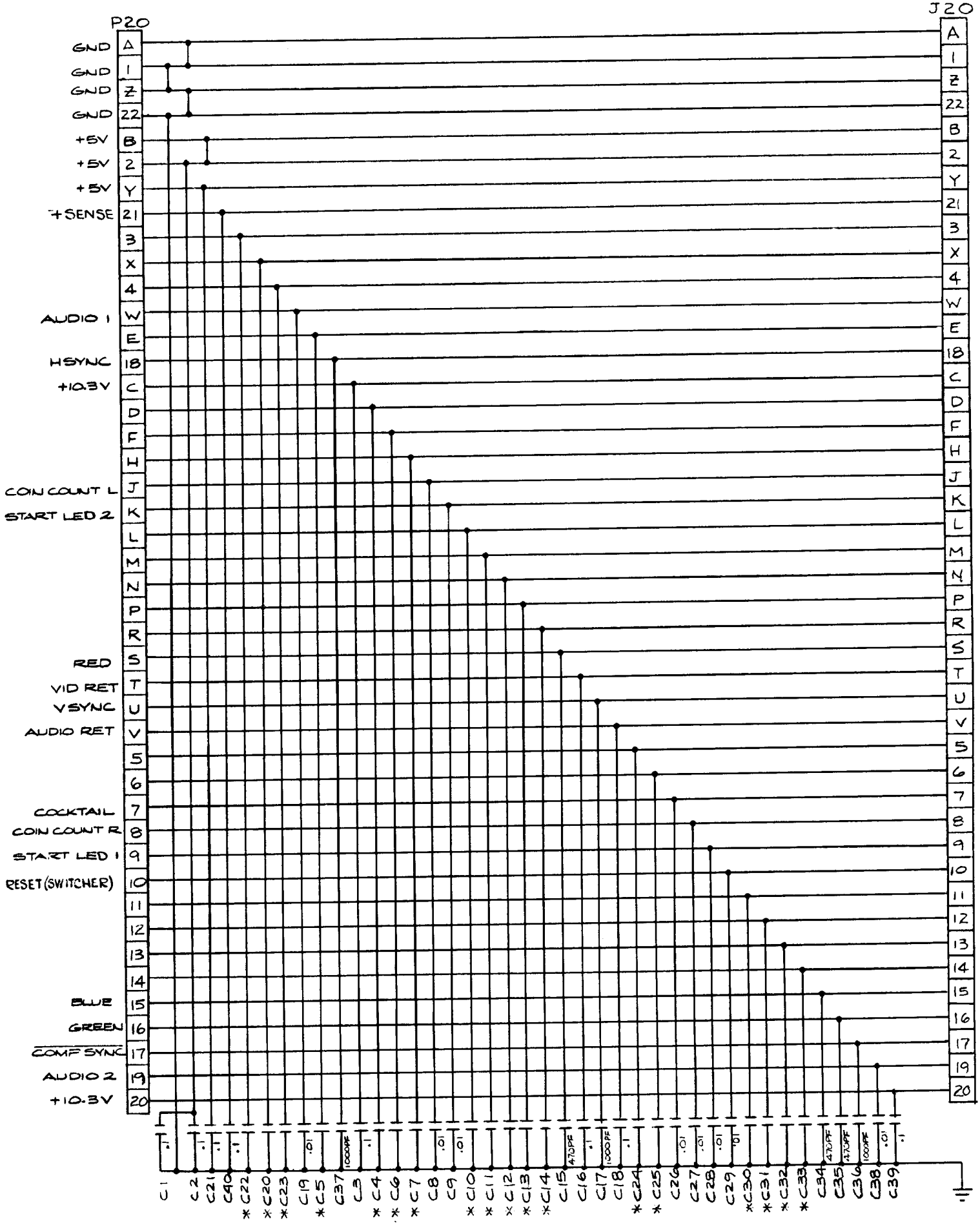
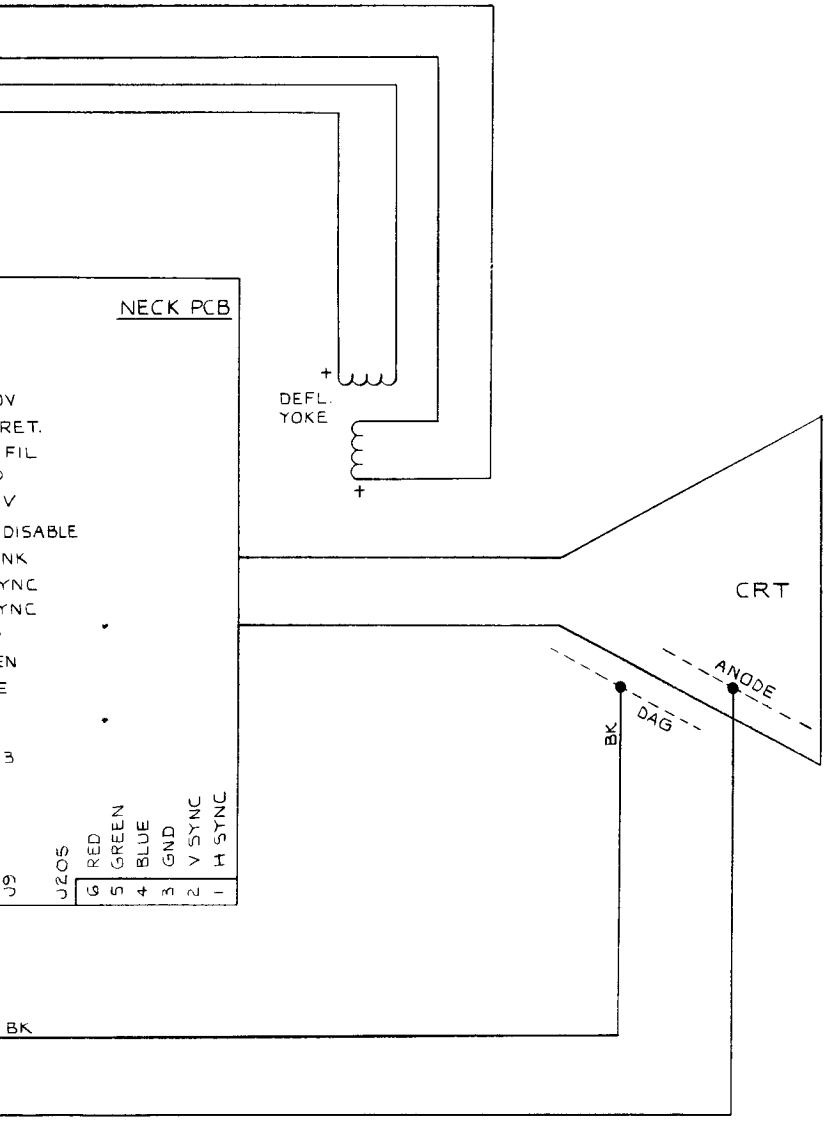

P20
J20
GND
GND
GND
GND
+5V
+5V
+5V
+SENSE
AUDIO 1
HSYNC
+10.3V
COIN COUNT L
START LED 2
RED
VID RET
VSYNC
AUDIO RET
COCKTAIL
COIN COUNT R
START LED 1
RESET (SWITCHER)
BLUE
GREEN
COMP SYNC
AUDIO 2
+10.3V
C1 .1
C2 .1
C21 .1
C40 .1
*C22 .1
*C20 .1
*C23 .1
C19 .01
*C5 .01
C37 1000PF
C3 .1
*C4 .1
*C6 .1
*C7 .1
C8 .01
C9 .01
*C10 .01
*C11 .1
*C12 .1
*C13 .1
*C14 .1
C15 470PF
C16 .1
C17 1000PF
C18 .1
*C24 .1
*C25 .1
C26 .01
C27 .01
C28 .01
C29 .01
*C30 .1
*C31 .1
*C32 .1
*C33 .1
C34 470PF
C35 470PF
C36 1000PF
C38 .01
C39 .1



NOTE:

1. ALTERNATE COLOR IN PARENTHESES ( ).

Atari Color Raster Display Wiring Diagram

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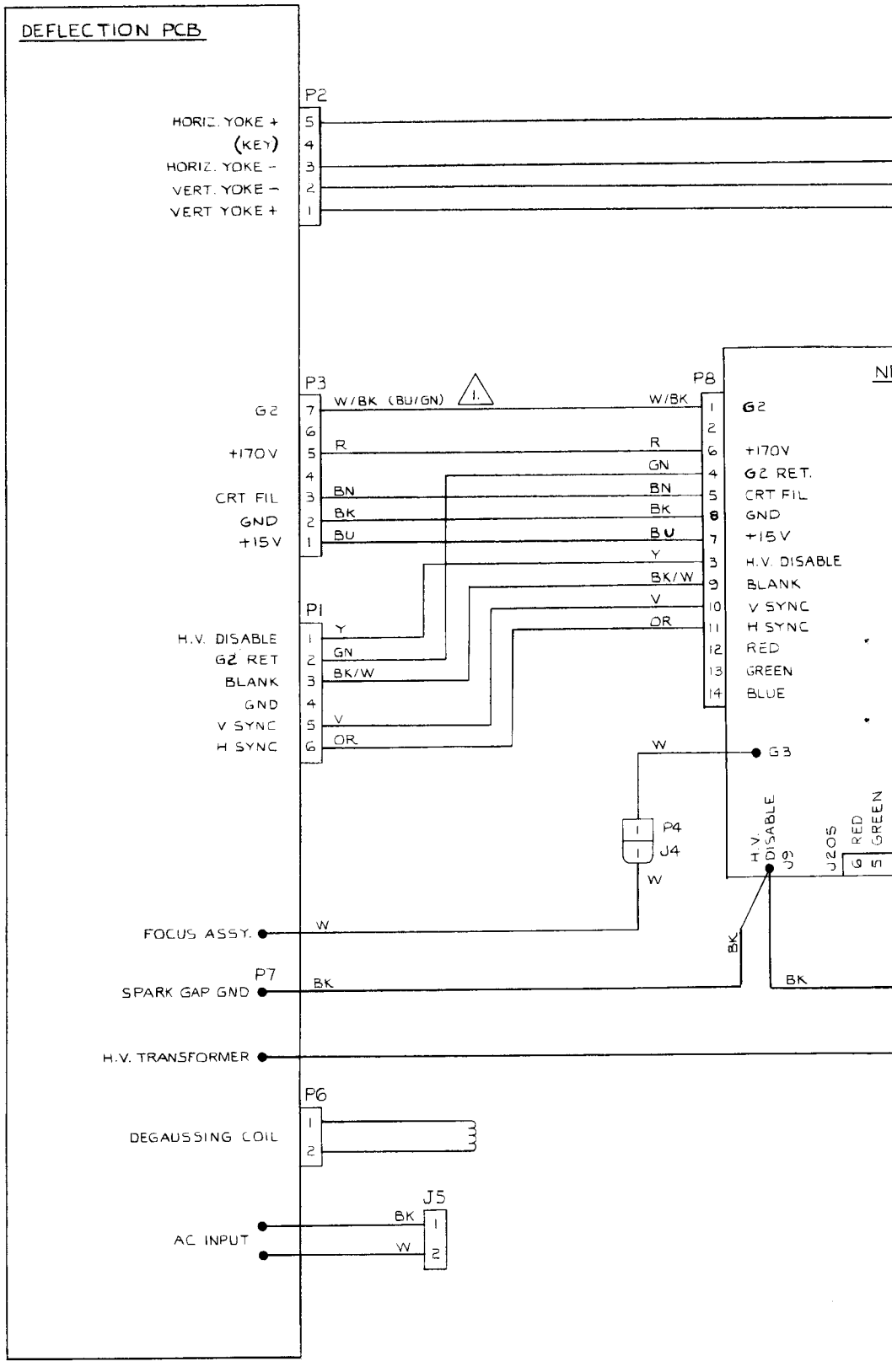
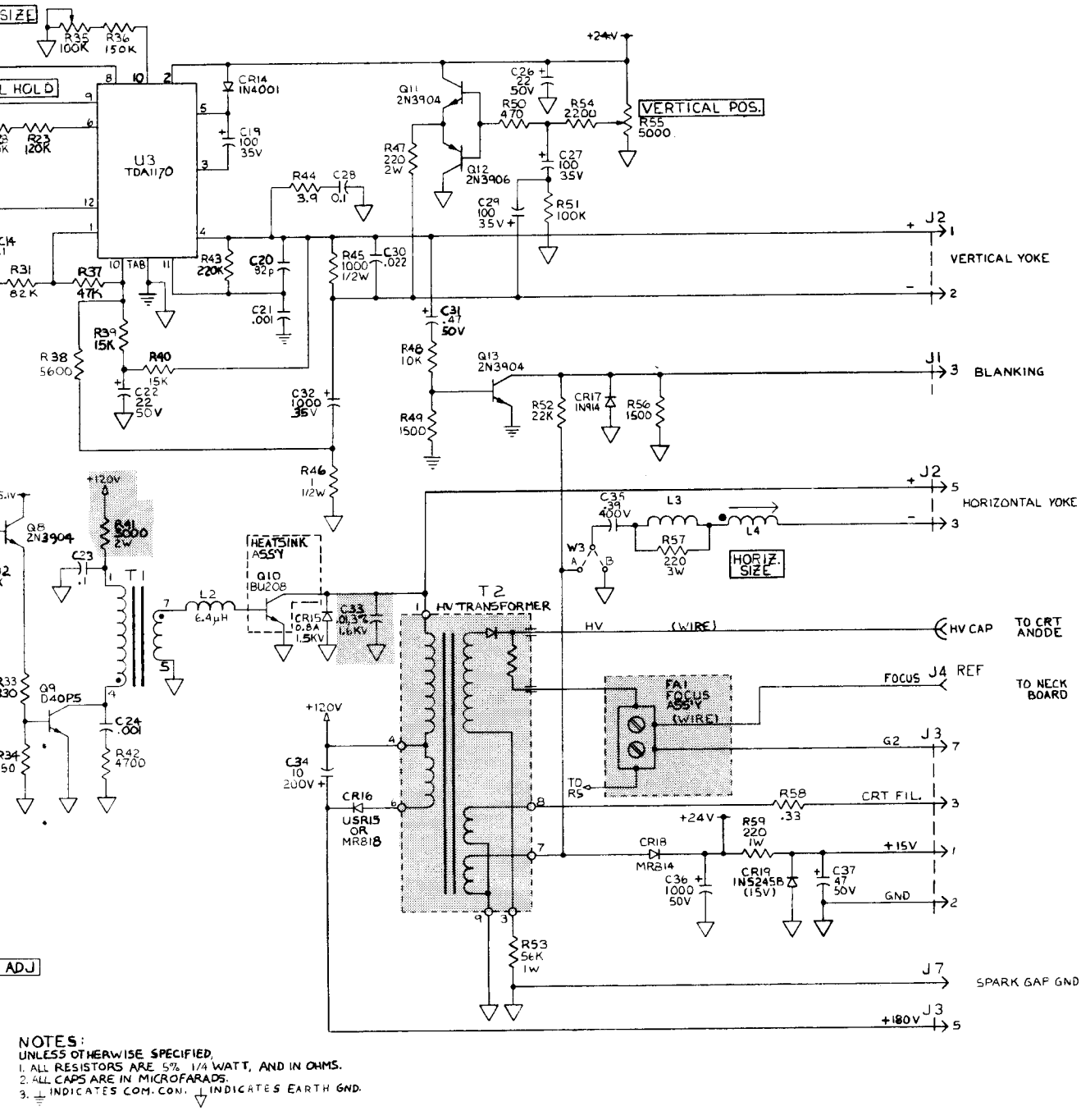
1st printing


DEFLECTION PCB
P2
HORIZ. YOKE +
(KEY)
HORIZ. YOKE –
VERT. YOKE –
VERT YOKE +
P3
G2
+170V
CRT FIL
GND
+15V
W/BK (BU/GN)
1.
P1
H.V. DISABLE
G2 RET
BLANK
GND
V SYNC
H SYNC
P8
W/BK
R
GN
BN
BK
BU
Y
BK/W
V
OR
G2
+170V
G2 RET.
CRT FIL
GND
+15V
H.V. DISABLE
BLANK
V SYNC
H SYNC
RED
GREEN
BLUE
G3
P4
J4
H.V. DISABLE J9
J205
RED
GREEN
FOCUS ASSY.
P7
SPARK GAP GND
H.V. TRANSFORMER
P6
DEGAUSSING COIL
J5
AC INPUT



NOTES:
UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTORS ARE 5% 1/4 WATT, AND IN OHMS.
2. ALL CAPS ARE IN MICROFARADS.
3. ⏚ INDICATES COM. CON. ⏚ INDICATES EARTH GND.

PRODUCT SAFETY NOTICE

The shaded areas of this schematic indicate components whose values are of special significance to product safety. Should any component in the shaded areas need to be replaced, use only the value given in the parts lists. Do not deviate from the resistance, wattage, and voltage values shown.

Atari Color Raster Display Deflection PCB

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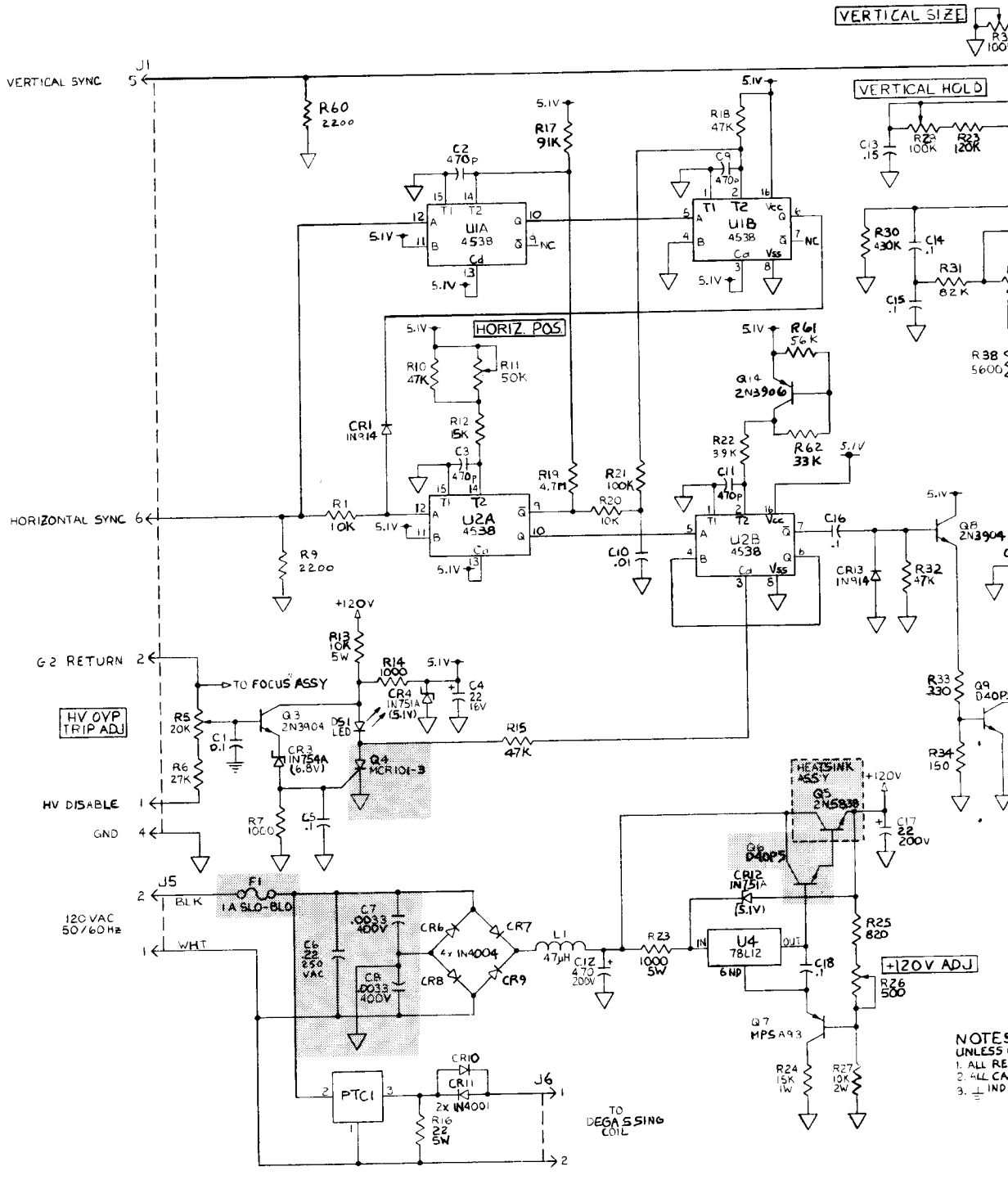
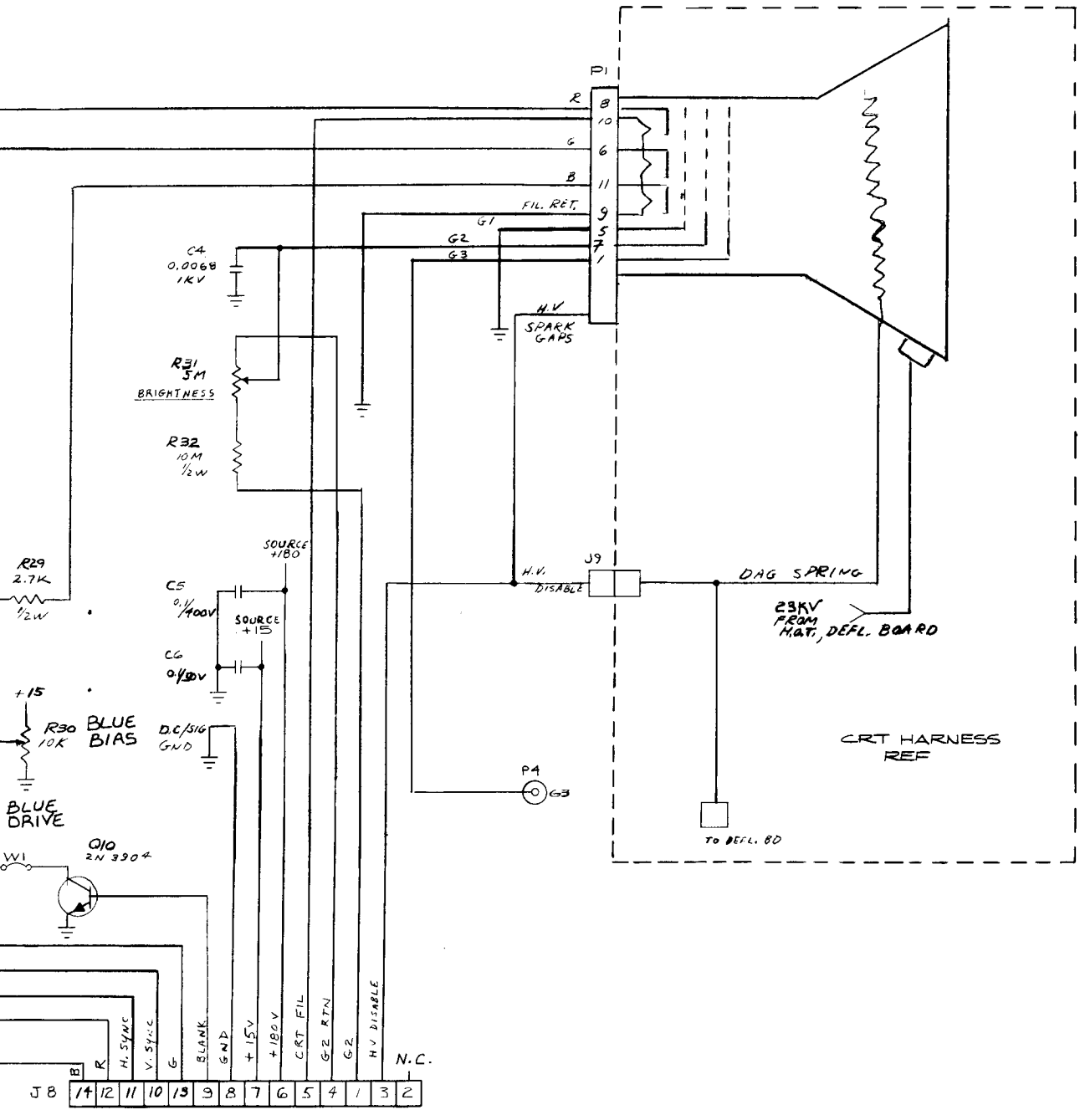

VERTICAL SIZE
VERTICAL HOLD
VERTICAL SYNC
HORIZONTAL SYNC
G2 RETURN
HV OVP TRIP ADJ
HV DISABLE
GND
120 VAC 50/60Hz
HORIZ POS
+120V
+120V ADJ
HEATSINK ASSY
TO FOCUS ASSY
TO DEGASSING COIL
NOTES
UNLESS



Atari Color Raster Display Neck PCB

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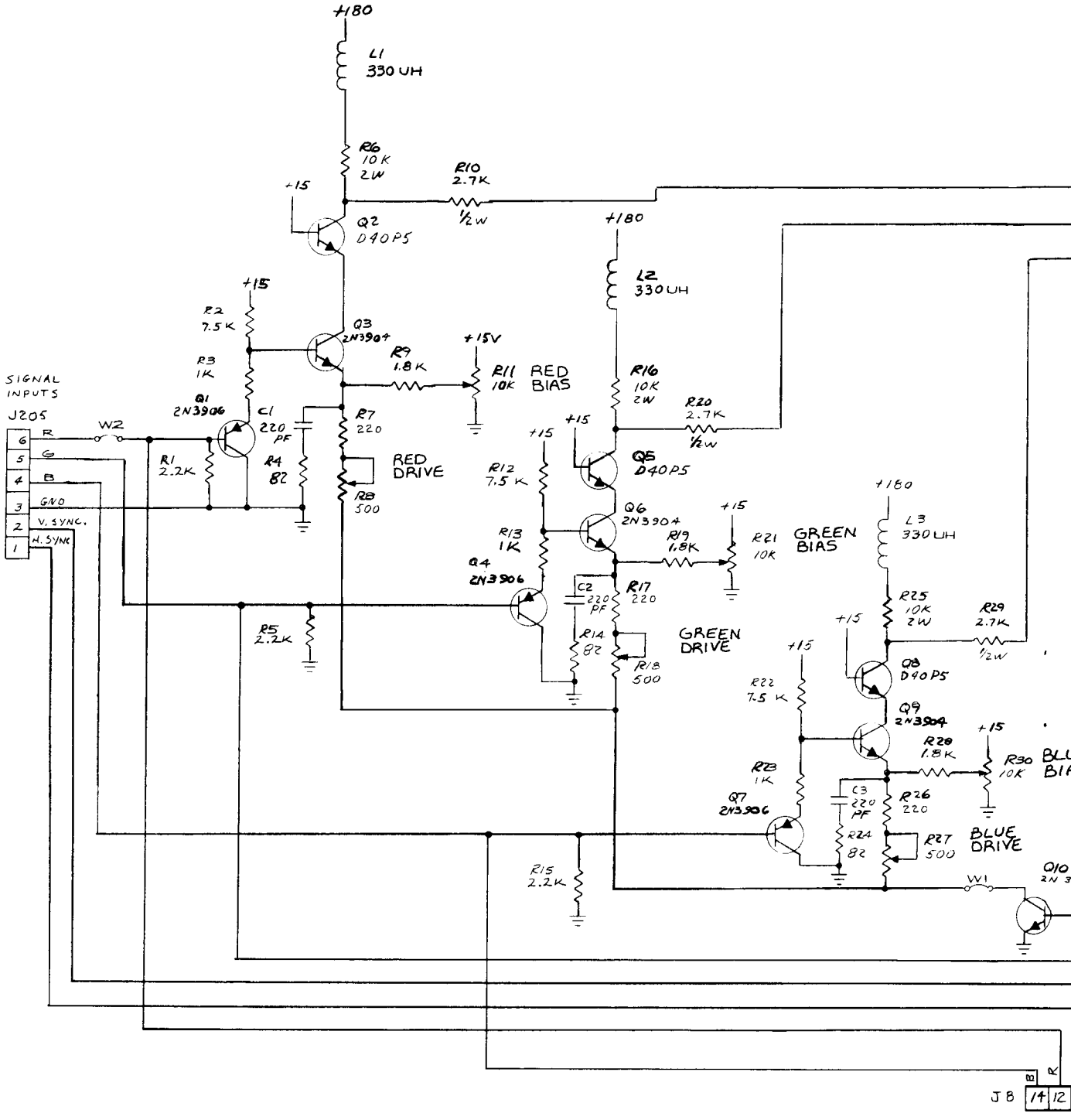
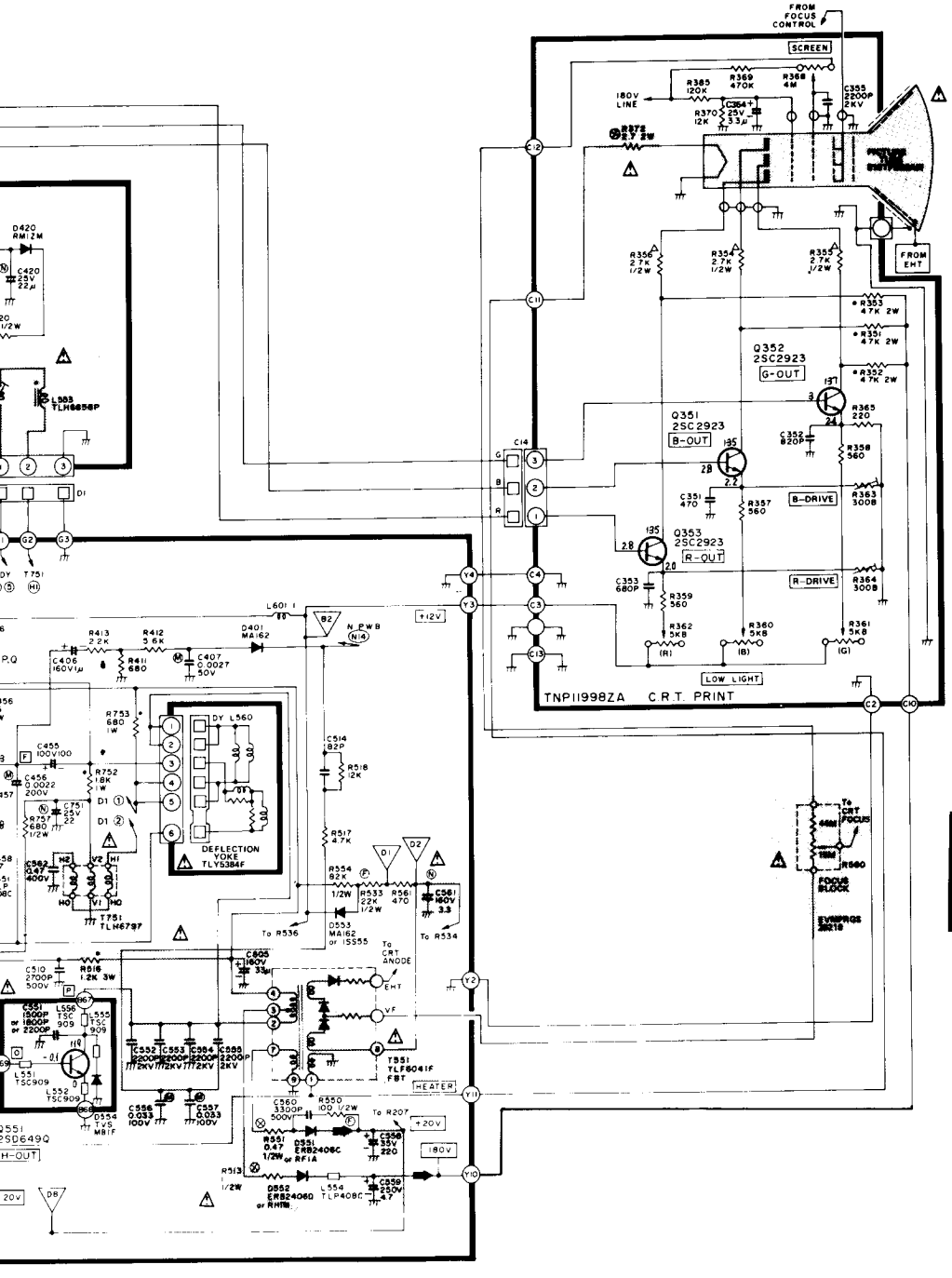
Sp-241 Sheet 10B
1st printing


+180
L1
330 UH
R6
10K
2W
R10
2.7K
1/2W
+15
Q2
D40P5
+180
L2
330UH
+15
R2
7.5K
Q3
2N3904
R3
1K
R9
1.8K
+15V
R11
10K
RED
BIAS
R16
10K
2W
R20
2.7K
1/2W
SIGNAL
INPUTS
J205
6 R
5 G
4 B
3 GND
2 V. SYNC.
1 H. SYNC
W2
Q1
2N3906
C1
220
PF
R7
220
R1
2.2K
R4
82
RED
DRIVE
R8
500
+15
R12
7.5K
Q5
D40P5
+180
Q6
2N3904
+15
R13
1K
R19
1.8K
R21
10K
GREEN
BIAS
L3
330UH
Q4
2N3906
C2
220
PF
R17
220
R5
2.2K
R14
82
R18
500
GREEN
DRIVE
+15
R25
10K
2W
R29
2.7K
1/2W
Q8
D40P5
+15
R22
7.5K
Q9
2N3904
+15
R28
1.8K
R30
10K
BLU
BIA
R23
1K
Q7
2N3906
C3
220
PF
R26
220
R24
82
R27
500
BLUE
DRIVE
R15
2.2K
W1
Q10
2N 3
J8
B
R
14
12



WARNING

Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.

Matsushita Color Raster Display

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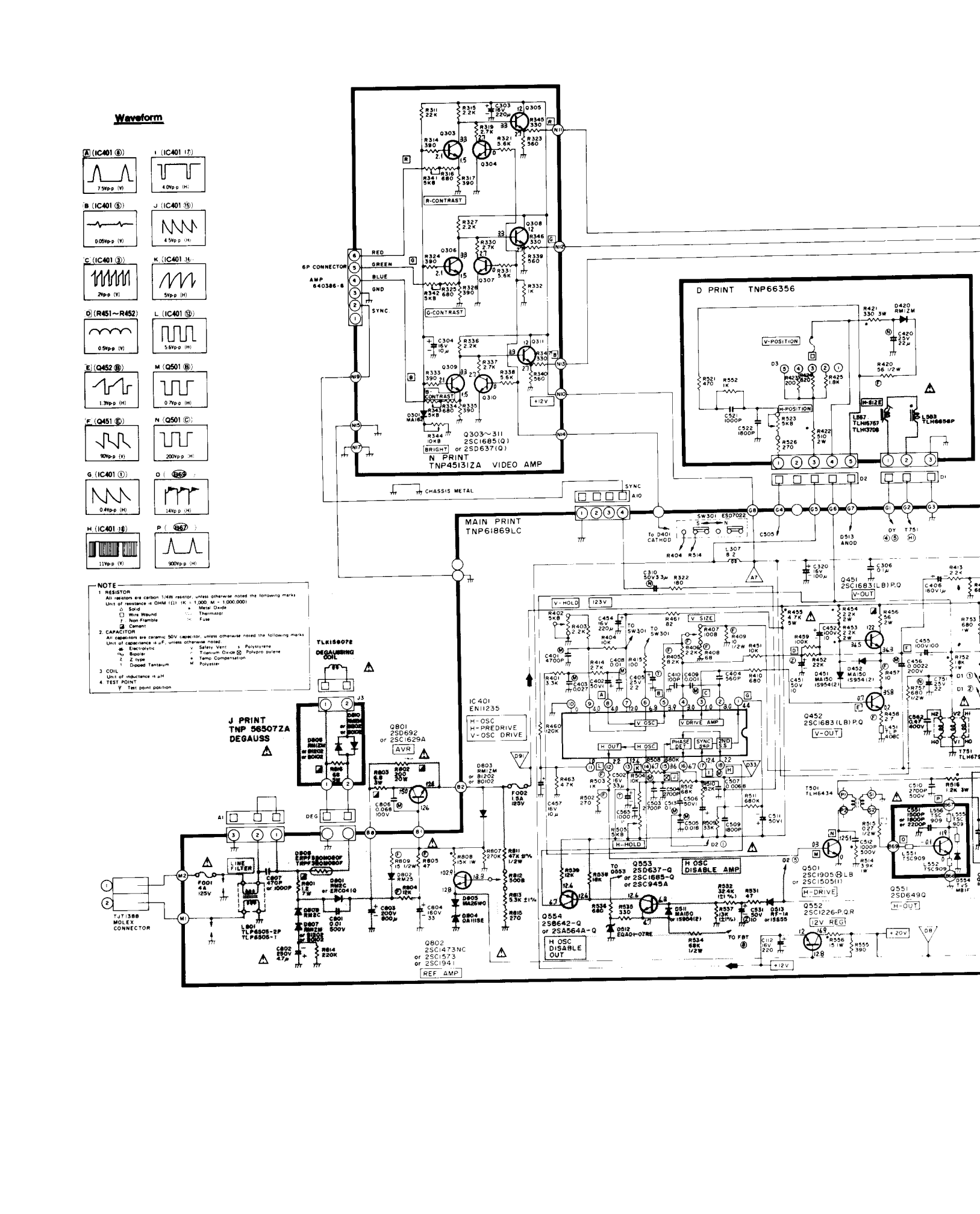
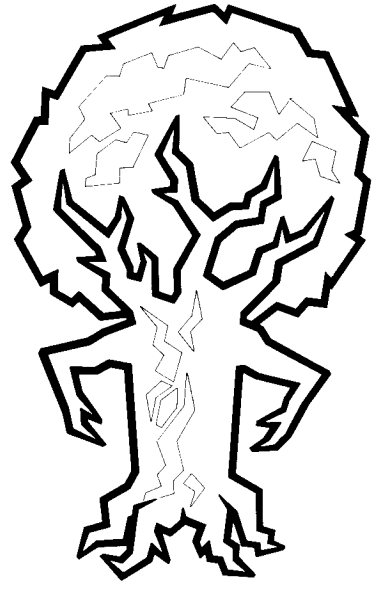
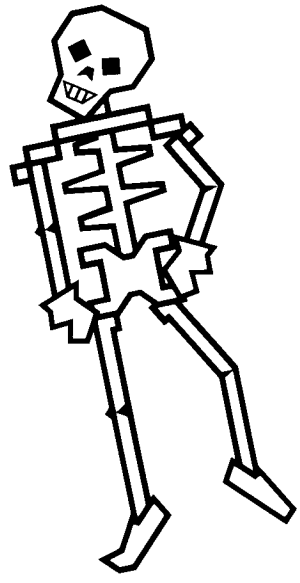

Waveform
A (IC401 ⑧)
7.5Vp-p (V)
I (IC401 ⑰)
4.0Vp-p (H)
B (IC401 ⑤)
0.05Vp-p (V)
J (IC401 ⑮)
4.5Vp-p (H)
C (IC401 ③)
2Vp-p (V)
K (IC401 ⑯)
5Vp-p (H)
D (R451~R452)
0.5Vp-p (V)
L (IC401 ⑫)
5.6Vp-p (H)
E (Q452 ⑧)
1.3Vp-p (H)
M (Q501 ⑧)
0.7Vp-p (H)
F (Q451 ⑧)
90Vp-p (V)
N (Q501 ⑥)
200Vp-p (H)
G (IC401 ①)
0.4Vp-p (H)
O (D69)
14Vp-p (H)
H (IC401 ⑱)
11Vp-p (V)
P (D67)
900Vp-p (H)
NOTE
1. RESISTOR
All resistors are carbon 1/4W resistor, unless otherwise noted the following marks
Unit of resistance is OHM (Ω) (K = 1,000, M = 1,000,000)
Ω Solid
Wire Wound
F Non Flamble
Cement
Metal Oxide
Thermistor
Fuse
2. CAPACITOR
All capacitors are ceramic 50V capacitor, unless otherwise noted the following marks
Unit of capacitance is μF, unless otherwise noted.
Electrolytic
Bipolar
Z Z type
T Doped Tantalum
V Safety Vent
Titanium Oxide
Temp Compensation
Polyester
S Polystyrene
Polypro pylene
3. COIL
Unit of inductance is μH
4. TEST POINT
Test point position
R-CONTRAST
G-CONTRAST
B-CONTRAST
BRIGHT
6P CONNECTOR
AMP 640386-6
RED
GREEN
BLUE
GND
SYNC
Q303~311
2SC1685(Q)
or 2SD637(Q)
N PRINT
TNP45131ZA VIDEO AMP
+12V
CHASSIS METAL
D PRINT TNP66356
V-POSITION
H-POSITION
H-SIZE
MAIN PRINT
TNP61869LC
SW301 ESD7022
To D401 CATHOD
D513 ANOD
SYNC
V-HOLD
123V
V SIZE
V-OUT
Q451
2SC1683(LB)P,Q
Q452
2SC1683(LB)P,Q
V OSC
V DRIVE AMP
H OUT
H OSC
PHASE DET
SYNC SEP
2ND
H-HOLD
H OSC DISABLE AMP
H OSC DISABLE OUT
IC401
EN11235
H-OSC
H-PREDRIVE
V-OSC DRIVE
Q553
2SD637-Q
or 2SC1685-Q
or 2SC945A
Q554
2SB642-Q
or 2SA564A-Q
Q501
2SC1905⊕LB
or 2SC1505(1)
H-DRIVE
Q552
2SC1226-P,Q,R
12V REG
Q551
2SD649Q
H-OUT
TLK158072
DEGAUSSING COIL
J PRINT
TNP 56507ZA
DEGAUSS
Q801
2SD692
or 2SC1629A
AVR
Q802
2SC1473NC
or 2SC1573
or 2SC1941
REF AMP
TJT1388
MOLEX CONNECTOR
LINE FILTER
L801
TLP6505-2P
TLP6505-1
IC401
EN11235
H-OSC
H-PREDRIVE
V-OSC DRIVE





Crystal Castles™ Troubleshooting Guide

ATARI®

A Warner Communications Company

7M

SP-241
1st printing

Crystal Castles™ Troubleshooting with the CAT Box

Troubleshooting with the Read/Write Controller

A. CAT Box Preliminary Set-Up

1. Remove the electrical power from the game and the CAT Box.
2. Remove the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet.
4. Remove Microprocessor 2C from the game PCB.
5. Connect the harness from the game to the game PCB.
6. Connect together the Φ0 and Φ2 test points on the game PCB with the shortest possible jumper.
7. Connect the $\overline{\text{WDDIS}}$ test point to ground.
8. Connect the CAT Box flex cable to the game PCB edge test connector.
9. Apply power to the game and to the CAT Box.
10. Set CAT Box switches as indicated:
    a. TESTER SELF-TEST: OFF
    b. TESTER MODE: R/$\overline{\text{W}}$
11. Press TESTER RESET.
12. Connect the DATA PROBE to the CAT Box. Connect the DATA PROBE ground clip to a game PCB ground test point.

B. Checking the Address Lines

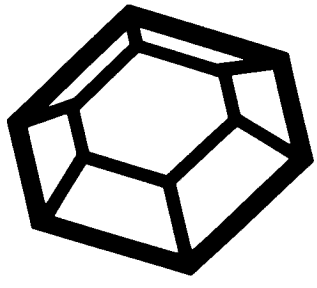
1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. BYTES: 1
    b. PULSE MODE: UNLATCHED
    c. R/$\overline{\text{W}}$ MODE: (OFF)
    d. R/$\overline{\text{W}}$: READ
3. Key in the address pattern given in Table 1 (use AAAA to start) with the CAT Box keyboard.
4. Set R/$\overline{\text{W}}$ MODE to STATIC.
5. Probe each IC-pin listed in Table 1 with the DATA PROBE and check that the CAT Box 1 or 0 LED for the corresponding address line lights up.
6. Repeat parts 2-c through 5 using address 5555 in part 3.

Table 1 Address Lines

Logic State for Address AAAA	IC-Pin	Logic State for Address 5555
BA15 1	1B3	0
BA14 0	1B5	1
BA13 1	1B7	0
BA12 0	1B9	1
BA11 1	1B12	0
BA10 0	1B14	1
BA9 1	1B16	0
BA8 0	1B18	1
BA7 1	1C9	0
BA6 0	1C7	1
BA5 1	1C5	0
BA4 0	1C3	1
BA3 1	1C12	0
BA2 0	1C14	1
BA1 1	1C16	0
BA0 0	1C18	1

C. Checking the Data Lines

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. BYTES:1
    b. R/$\overline{\text{W}}$ MODE: (OFF)
    c. R/$\overline{\text{W}}$: WRITE
3. Key in address 0000 with the keyboard.
4. Press DATA SET. Key in data AA with the keyboard.
5. Set R/$\overline{\text{W}}$ MODE to STATIC.
6. Probe each IC-pin listed in Table 2 with the DATA PROBE and check that the CAT Box 1 or 0 LED for the corresponding address line lights up.
7. Set R/$\overline{\text{W}}$ MODE to (OFF).
8. Repeat parts 4 through 6 using data 55 in part 4.



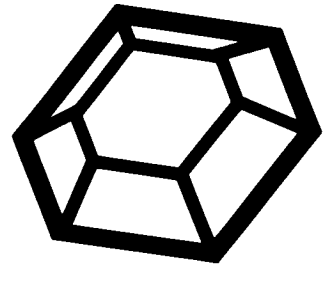


Table 2 Data Lines

Logic State for Data AA		IC-Pin	Logic State for Data 55
D7	1	2E-11	0
D6	0	2E-12	1
D5	1	2E-13	0
D4	0	2E-14	1
D3	1	2E-15	0
D2	0	2E-16	1
D1	1	2E-17	0
D0	0	2E-18	1
BD7	1	2E-9	0
BD6	0	2E-8	1
BD5	1	2E-7	0
BD4	0	2E-6	1
BD3	1	2E-5	0
BD2	0	2E-4	1
BD1	1	2E-3	0
BD0	0	2E-2	1

D. Checking the RAM

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: ADDR
   b. BYTES:1024
   c. R/$\overline{W}$ MODE: (OFF)
   d. R/$\overline{W}$: WRITE
3. Enter address 0003 with the keyboard.
4. Set the CAT Box switches as indicated:
   a. R/$\overline{W}$ MODE to PULSE and back to (OFF)
   b. R/$\overline{W}$ to READ
   c. R/$\overline{W}$ MODE to PULSE and back to (OFF)
5. If the CAT Box reads an address that doesn't compare with that written, the COMPARE ERROR LED will light up. The ADDRESS/SIGNATURE display of the CAT Box will show the failing address location and the ERROR DATA DISPLAY switch is enabled. Using this switch, determine if the error is in the high-order or low-order RAM.
6. Repeat this test with DBUS SOURCE set to ADDR.
7. Set the CAT Box switches as indicated:
   a. BYTES: 256
   b. DBUS SOURCE: ADDR
   c. R/$\overline{W}$: (OFF)
   d. R/$\overline{W}$: WRITE
8. Repeat parts 5 through 6 to check addresses from 1000 through 8FFF.

NOTE

The two custom audio I/O chips must be tested separately by performing the self-test, substituting a known good part, or performing the following procedure.

E. Checking the Custom Audio I/O Chips

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{W}$: WRITE
   c. R/$\overline{W}$ MODE: (OFF)
3. Enter the address from Table 3 with the keyboard.
4. Press DATA SET and enter the data from Table 3 with the keyboard.
5. Set R/$\overline{W}$ to PULSE and back to (OFF).
6. Repeat parts 3 through 5 for each address and data listed in Table 3. Check for the response indicated.

Table 3 Custom Audio I/O Chips

Address	Data	Test Results
98	00	Custom Audio I/O Chip 4D channel 1 produces pure tone.
98	03	
98	55	
98	AF	
98	00	Custom Audio I/O Chip 4D channel 1 turns off.
98	55	Custom Audio I/O Chip 4D channel 2 produces pure tone.
98	AF	
98	00	Custom Audio I/O Chip 4D channel 2 turns off.
9A	00	Custom Audio I/O Chip 4B channel 1 produces pure tone.
9A	03	
9A	55	
9A	AF	
9A	00	Custom Audio I/O Chip 4B channel 1 turns off.
9A	55	Custom Audio I/O Chip 4B channel 2 produces pure tone.
9A	AF	
9A	00	Custom Audio I/O Chip 4B channel 2 turns off.

F. Checking the Player Switch, Option Switch, and Trak-Ball™ Inputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{W}$: WRITE
   c. R/$\overline{W}$ MODE: (OFF)
3. Enter address 9600 with the keyboard.
4. Press DATA SET and enter data FF with the keyboard.
5. Set R/$\overline{WE}$ to PULSE and back to (OFF).
6. For each entry listed in Table 4, do the following:
   a. Set R/$\overline{W}$ MODE to (OFF).
   b. Set R/$\overline{W}$WRITE.
   c. Enter the first address with the keyboard.
   d. Press DATA SET and enter the data for that address with the keyboard.
   e. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
   f. Set R/$\overline{W}$ to READ.
   g. Enter the next address.
   h. Set R/$\overline{W}$ MODE to STATIC.
   i. Activate the input switch or signal indicated in Table 4 and check the test result.
   j. Set R/$\overline{W}$ MODE to (OFF).
   k. Repeat parts g through j for each subsequent address given for the entry.

Table 4 Player Switches, Option Switches, and Trak-Ball™ Inputs

Address	Input Switches/Signals	Test Results
9400	Trak-Ball™ VERT	
9401	Trak-Ball™ HORIZ	
9402	Trak-Ball™ VERT (Player 2)	
9403	Trak-Ball™ HORIZ (Player 2)	
9600	D0 COIN R	
	D1 COIN L	
	D2 COIN AUX	
	D3 SLAM	
	D4 SELF TEST	
	D5 SPARE	
	D6 JMP1	
	D7 JMP2	
00–9A0B	SW2 D0	Read switches at address 9A08. DATA display changes when any of these switches or signals are activated.
	SW3 D1	
	SW4 D2	

G. Checking the Coin Counter and Trak-Ball Light

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES: 1
   c. R/$\overline{W}$: WRITE
   d. R/$\overline{W}$ MODE: (OFF)
3. Enter the address in Table 5 with the keyboard.

CAUTION

If you write ON data to activate a solenoid, *deactivate the solenoid immediately* by writing the OFF data. If you leave a solenoid activated for more than 10 seconds, you may have to replace the solenoid and/or its driver, due to overheating.

4. For each address listed in Table 5, do the following:
   a. To activate the output:
      - Press DATA SET.
      - Enter the ON data with the keyboard.
      - Set R/$\overline{W}$ MODE to STATIC and back to (OFF).
   b. To deactivate the output:
      - Press DATA SET.
      - Enter the OFF data with the keyboard.
      - Set R/$\overline{W}$ MODE to STATIC and back to (OFF).

Table 5 LED and Coin Counter Outputs

Address	On Data	Off Data	Output Device
9E86	FF	00	Left Coin Counter
9E85	FF	00	Right Coin Counter
9E80	FF	00	Trak-Ball™ Light

Troubleshooting the Watchdog Circuit

The Watchdog circuit will send continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuit. If the self-test fails to run, it is a good practice to check the RESET line.

$\overline{\text{RESET}}$ is a microprocessor input (pin 40). In a properly operating game, reset should occur during power-up or when the $\overline{\text{RESET}}$ test point is grounded. A pulsing $\overline{\text{RESET}}$ line indicates that something is causing the microprocessor to lose its place within the program. Typical causes are:

1. Open or shorted address or data bus lines.
2. Bad microprocessor chip.
3. Bad bus buffers.
4. Bad ROM.
5. Bad RAM.
6. Any bad input or output that causes an address or data line to be held in a constant high or low state.

A pulsing $\overline{\text{RESET}}$ signal indicates a problem exists somewhere within the microprocessor circuitry. To aid in troubleshooting, the $\overline{\text{WDDIS}}$ test point can be connected to a ground test point to prevent resets. This will sometimes allow the Self-Test to be used to diagnose the failure during a RESET condition.